CHAPTER 2

DIGITAL MODULATION

2.1 INTRODUCTION

Referring to Equation (2.1), if the information signal is digital and the amplitude (lV of the carrier is varied proportional to the information signal, a digitally modulated signal called *amplitude shift keying* (ASK) is produced.

If the frequency (f) is varied proportional to the information signal, *frequency shift keying* (FSK) is produced, and if the phase of the carrier (0) is varied proportional to the information signal, *phase shift keying (PSK) is* produced.

If both the amplitude and the phase are varied proportional to the information signal, *quadrature amplitude modulation* (QAM) results. ASK, FSK, PSK, and QAM are all forms of digital modulation:

$$v(t) = V \sin(2\pi \cdot ft + \theta) \qquad (2.1)$$

ASK FSK PSK

QAM

Figure 2-1 shows a simplified block diagram for a digital modulation system.

In the transmitter, the precoder performs level conversion and then encodes the incoming data into groups of bits that modulate an analog carrier.

The modulated carrier is shaped (filtered), amplified, and then transmitted through the transmission medium to the receiver.

The transmission medium can be a metallic cable, optical fiber cable, Earth's atmosphere, or a combination of two or more types of transmission systems.

In the receiver, the incoming signals are filtered, amplified, and then applied to the demodulator and decoder circuits, which extracts the original source information from the modulated carrier.

The clock and carrier recovery circuits recover the analog carrier and digital timing (clock) signals from the incoming modulated wave since they are necessary to perform the de-modulation process.

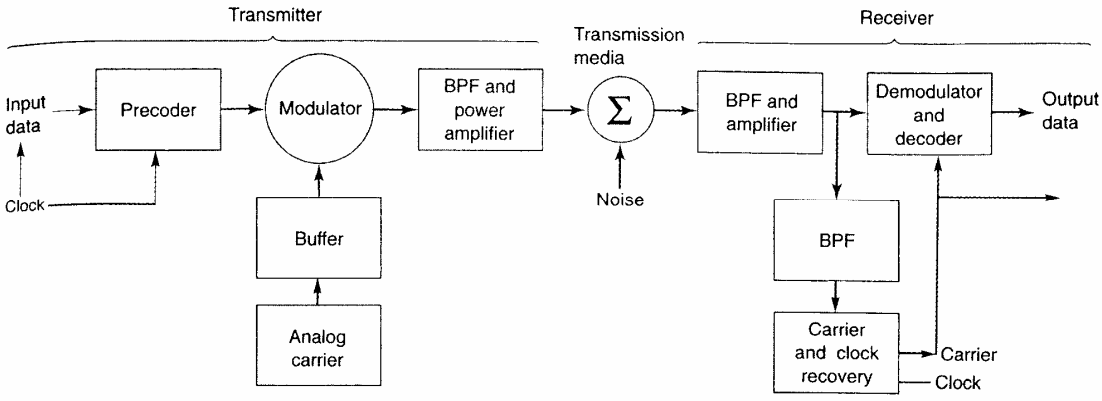


FIGURE 2-1 Simplified block diagram of a digital radio system.

2-2 INFORMATION CAPACITY, BITS, BIT RATE, BAUD, AND MARY ENCODING

2-2-1 Information Capacity, Bits, and Bit Rate

$$I \propto B \times t \qquad (2.2)$$

where I= information capacity (bits per second)
B = bandwidth (hertz)
t = transmission time (seconds)

From Equation 2-2, it can be seen that information capacity is a linear function of bandwidth and transmission time and is directly proportional to both.

If either the bandwidth or the transmission time changes, a directly proportional change occurs in the information capacity.

The higher the signal-to-noise ratio, the better the performance and the higher the information capacity.

Mathematically stated, *the Shannon limit_for information capacity is*

$$I = B \log_2\left(1 + \frac{S}{N}\right) \qquad (2.3)$$

or

$$I = 3.32B \log_{10}\left(1 + \frac{S}{N}\right) \qquad (2.4)$$

where I = information capacity (bps)
B = bandwidth (hertz)
$\frac{S}{N}$ = signal-to-noise power ratio (unitless)

For a standard telephone circuit with a signal-to-noise power ratio of 1000 (30 dB) and a bandwidth of 2.7 kHz, the Shannon limit for information capacity is

$$I = (3.32)(2700)\log_{10}(1 + 1000) = 26.9 \text{ kbps}$$

Shannon's formula is often misunderstood. The results of the preceding example indicate that 26.9 kbps can be propagated through a 2.7-kHz communications channel. This may be true, but it cannot be done with a binary system. To achieve an information transmission rate of 26.9 kbps through a 2.7-kHz channel, each symbol transmitted must contain more than one bit.

2-2-2 M-ary Encoding

M-ary is a term derived from the word *binary.*

M simply represents a digit that corresponds to the number of conditions, levels, or combinations possible for a given number of binary variables.

For example, a digital signal with four possible conditions (voltage levels, frequencies, phases, and so on) is an M-ary system where M = 4. If there are eight possible conditions, M = 8 and so forth.

The number of bits necessary to produce a given number of conditions is expressed mathematically as

$$N = \log_2 M \tag{2.5}$$

where N = number of bits necessary
M = number of conditions, levels, or combinations

possible with *N* bits

Equation 2-5 can be simplified and rearranged to express the number of conditions possible with *N* bits as

$$2^N = M \tag{2.6}$$

For example, with one bit, only $2^1 = 2$ conditions are possible. With two bits, $2^2 = 4$ conditions are possible, with three bits, $2^3 = 8$ conditions are possible, and so on.

2-2-3 Baud and Minimum Bandwidth

Baud refers to the rate of change of a signal on the transmission medium after encoding and modulation have occurred.

Hence, baud is a unit of transmission rate, modulation rate, or symbol rate and, therefore, the terms symbols per second and baud are often used interchangeably.

Mathematically, baud is the reciprocal of the time of one output signaling element, and a signaling element may represent several information bits. Baud is expressed as

$$\text{baud} = \frac{1}{t_s} \tag{2.7}$$

where baud = symbol rate (baud per second)

t_s = time of one signaling element (seconds)

The minimum theoretical bandwidth necessary to propagate a signal is called the minimum Nyquist bandwidth or sometimes the minimum Nyquist frequency.

Thus, $f_b = 2B$, where f_b is the bit rate in bps and B is the ideal Nyquist bandwidth.

The relationship between bandwidth and bit rate also applies to the opposite situation. For a given bandwidth (B), the highest theoretical bit rate is 2B.

For example, a standard telephone circuit has a bandwidth of approximately 2700 Hz, which has the capacity to propagate 5400 bps through it. However, if more than two levels are used for signaling (higher-than-binary encoding), more than one bit may be transmitted at a time, and it is possible to propagate a bit rate that exceeds 2B.

Using multilevel signaling, the Nyquist formulation for channel capacity is

$$f_b = B \log_2 M \qquad (2.8)$$

where f_b = channel capacity (bps)

B = minimum Nyquist bandwidth (hertz)

M = number of discrete signal or voltage levels

Equation 2.8 can be rearranged to solve for the minimum bandwidth necessary to pass M-ary digitally modulated carriers

$$B = \left(\frac{f_b}{\log_2 M} \right) \qquad (2.9)$$

If N is substituted for $\log_2$ M, Equation 2.9 reduces to

$$B = \left(\frac{f_b}{N} \right) \tag{2.10}$$

where N is the number of bits encoded into each signaling element.

In addition, since baud is the encoded rate of change, it also equals the bit rate divided by the number of bits encoded into one signaling element. Thus,

$$\text{Baud} = \left(\frac{f_b}{N} \right) \tag{2.11}$$

By comparing Equation *2.10* with Equation *2.11* the baud and the ideal minimum Nyquist bandwidth have the same value and are equal to the bit rate divided by the number of bits encoded.

2-3 AMPLITUDE-SHIFT KEYING

The simplest digital modulation technique is *amplitude-shift keying* (ASK), where a binary information signal directly modulates the amplitude of an analog carrier.

ASK is similar to standard amplitude modulation except there are only two output amplitudes possible. Amplitude-shift keying is sometimes called *digital amplitude modulation* (DAM).

Mathematically, amplitude-shift keying is

$$v_{(ask)}(t) = [1 + v_m(t)]\left[\frac{A}{2}\cos(\omega_c t)\right] \qquad (2.12)$$

where
$v_{ask}(t)$ = amplitude-shift keying wave
$v_m(t)$ = digital information (modulating) signal (volts)
A/2 = unmodulated carrier amplitude (volts)
ω_c = analog carrier radian frequency (radians per second, $2\pi f_c t$)

In Equation *2.12,* the modulating signal $[v_m(t)]$ *is* a normalized binary waveform, where + 1 V = logic 1 and -1 V = logic 0. Therefore, for a logic 1 input, $v_m(t)$ = + 1 V, Equation *2.12* reduces to

$$v_{(ask)}(t) = [1 + 1]\left[\frac{A}{2}\cos(\omega_c t)\right]$$

$$= A\cos(\omega_c t)$$

and for a logic 0 input, $v_m(t)$ = -1 V, Equation *2.12* reduces to

$$v_{(ask)}(t) = [1 - 1]\left[\frac{A}{2}\cos(\omega_c t)\right]$$

Thus, the modulated wave $v_{ask}(t)$, is either A $\cos(\omega_c t)$ or 0. Hence, the carrier is either *"on"*or *"off,"* which is why amplitude-shift keying is sometimes referred to as *on-off keying*(OOK).

Figure 2-*2* shows the input and output waveforms from an ASK modulator.

From the figure, it can be seen that for every change in the input binary data stream, there is one change in the ASK waveform, and the time of one bit *(t_b)* equals the time of one analog signaling element (t,).

$B = f_b / 1 = f_b$ baud $= f_b / 1 = f_b$

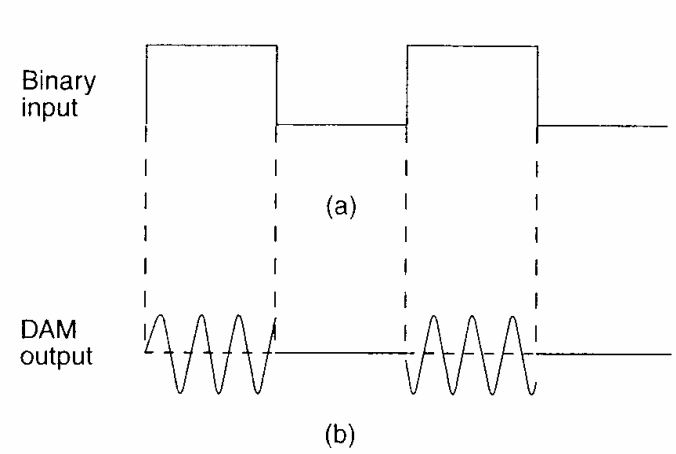


FIGURE 2-2 Digital amplitude modulation: (a) input binary; (b) output DAM waveform

The entire time the binary input is high, the output is a constant-amplitude, constant-frequency signal, and for the entire time the binary input is low, the carrier is off.

The rate of change of the ASK waveform (baud) is the same as the rate of change of the binary input (bps).

Example 2-1

Determine the baud and minimum bandwidth necessary to pass a 10 kbps binary signal using amplitude shift keying.

Solution

For ASK, N = 1, and the baud and minimum bandwidth are determined from Equations 2.11 and 2.10, respectively:

$$B = 10{,}000 / 1 = 10{,}000$$

$$\text{baud} = 10,000 / 1 = 10{,}000$$

The use of amplitude-modulated analog carriers to transport digital information is a relatively low-quality, low-cost type of digital modulation and, therefore, is seldom used except for very low-speed telemetry circuits.

2-4 FREQUENCY-SHIFT KEYING

FSK is a form of constant-amplitude angle modulation similar to standard frequency modulation (FM) except the modulating signal is a binary signal that varies between two discrete voltage levels rather than a continuously changing analog waveform.

Consequently, FSK is sometimes called *binary FSK* (BFSK). The general expression for FSK is

$$v_{fsk}(t) = V_c \cos\{2\pi[f_c + v_m(t)\,\Delta f]t\} \qquad (2.13)$$

where

$v_{fsk}(t)$ = binary FSK waveform
V_c = peak analog carrier amplitude (volts)
f_c = analog carrier center frequency (hertz)
Δf = peak change (shift) in the analog carrier frequency

(hertz)
$v_m(t)$ = binary input (modulating) signal (volts)

From Equation 2.13, it can be seen that the peak shift in the carrier frequency (Δf) is proportional to the amplitude of the binary input signal ($v_m[t]$), and the direction of the shift is determined by the polarity.

The modulating signal is a normalized binary waveform where a logic 1 = + 1 V and a logic 0 = -1 V. Thus, for a logic l input, $v_m(t)$ = + 1, Equation 2.13 can be rewritten as

$$v_{fsk}(t) = V_c \cos[2\pi(f_c + \Delta f)t]$$

For a logic 0 input, $v_m(t)$ = -1, Equation 2.13 becomes

$$v_{fsk}(t) = V_c \cos[2\pi(f_c - \Delta f)t]$$

With binary FSK, the carrier center frequency (f_c) is shifted (deviated) up and down in the frequency domain by the binary input signal as shown in Figure 2-3.

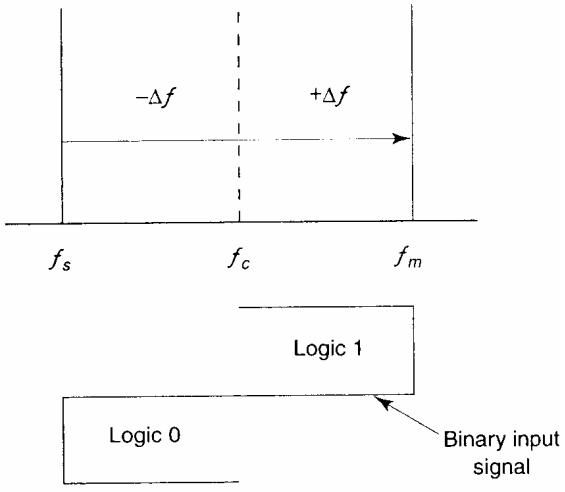


FIGURE 2-3 FSK in the frequency domain

As the binary input signal changes from a logic 0 to a logic 1 and vice versa, the output frequency shifts between two frequencies: a mark, or logic 1 frequency (f_m), and a space, or logic 0 frequency (f_s). The mark and space frequencies are separated from the carrier frequency by the peak frequency deviation (Δf) and from each other by 2 Δf.

Frequency deviation is illustrated in Figure 2-3 and expressed mathematically as

$$\Delta f = |f_m - f_s| / 2 \qquad (2.14)$$

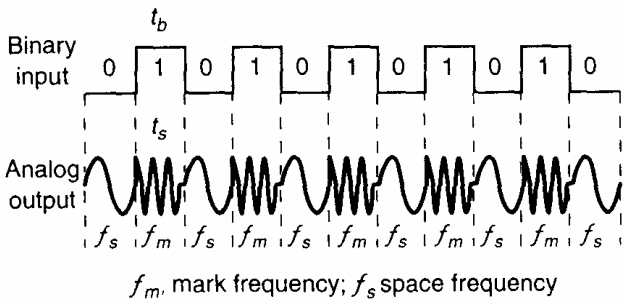
where Δf = frequency deviation (hertz)
$|f_m - f_s|$ = absolute difference between the mark and space frequencies (hertz)

Figure 2-4a shows in the time domain the binary input to an FSK modulator and the corresponding FSK output.

When the binary input *(f_b)* changes from a logic 1 to a logic 0 and vice versa, the FSK output frequency shifts from a mark (f_m) to a space (f_s) frequency and vice versa.

In Figure 2-4a, the mark frequency is the higher frequency *(f_c* + Δf) and the space frequency is the lower frequency (f_c - Δf), although this relationship could be just the opposite.

Figure 2-4b shows the truth table for a binary FSK modulator. The truth table shows the input and output possibilities for a given digital modulation scheme.



binary input	frequency output
0	space (f_s)
1	mark (f_m)

(b)

FIGURE 2-4 FSK in the time domain: (a) waveform: (b) truth table

2-4-1 FSK Bit Rate, Baud, and Bandwidth

In Figure 2-4a, it can be seen that the time of one bit *(t_b)* is the same as the time the FSK output is a mark of space frequency *(t_s)*. Thus, the bit time equals the time of an FSK signaling element, and the bit rate equals the baud.

The baud for binary FSK can also be determined by substituting N = 1 in Equation 2.11:

$$\text{baud} = f_b / 1 = f_b$$

The minimum bandwidth for FSK is given as

$$B = |(f_s - f_b) - (f_m - f_b)|$$
$$= |(f_s - f_m)| + 2f_b$$

and since $|(f_s - f_m)|$ equals $2\Delta f$, the minimum bandwidth can be approximated as

$$B = 2(\Delta f + f_b) \qquad (2.15)$$

where

B= minimum Nyquist bandwidth (hertz)
Δf= frequency deviation $|(f_m - f_s)|$ (hertz)
f_b = input bit rate (bps)

Example 2-2

Determine (a) the peak frequency deviation, (b) minimum bandwidth, and (c) baud for a binary FSK signal with a mark frequency of 49 kHz, a space frequency of 51 kHz, and an input bit rate of 2 kbps.

Solution

a. The peak frequency deviation is determined from Equation 2.14:

$$\Delta f = |149\text{kHz} - 51\text{ kHz}| / 2 = 1\text{ kHz}$$

b. The minimum bandwidth is determined from Equation 2.15:

$$B = 2(1000 + 2000)$$
$$= 6\text{ kHz}$$

c. For FSK, $N = 1$, and the baud is determined from Equation 2.11 as

$$\text{baud} = 2000 / 1 = 2000$$

Bessel functions can also be used to determine the approximate bandwidth for an FSK wave. As shown in Figure 2-5, the fastest rate of change (highest fundamental frequency) in a non-return-to-zero (NRZ) binary signal occurs when alternating 1s and 0s are occurring (i.e., a square wave).

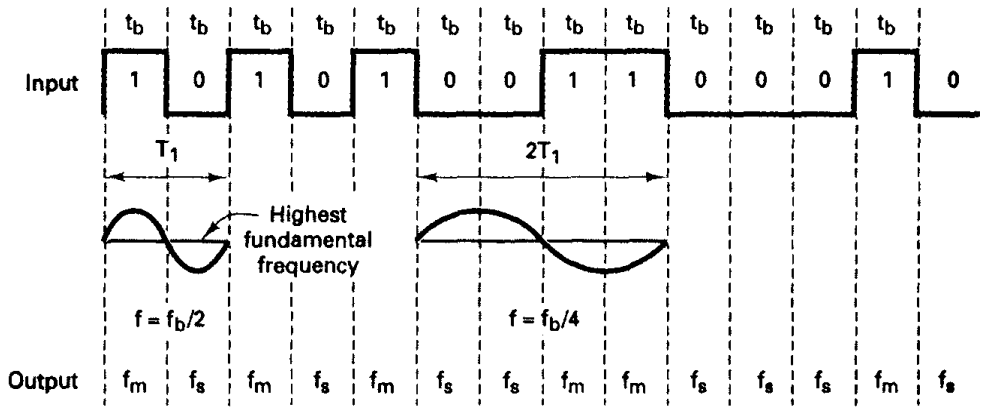


FIGURE 9-5 FSK modulator, t_b, time of one bit = $1/f_b$; f_m mark frequency; f_s, space frequency; T_1, period of shortest cycle; $1/T_1$, fundamental frequency of binary square wave; f_b, input bit rate (bps)

Since it takes a high and a low to produce a cycle, the highest fundamental frequency present in a square wave equals the repetition rate of the square wave, which with a binary signal is equal to half the bit rate. Therefore,

$$f_a = f_b / 2 \qquad (2.16)$$

where
f_a = highest fundamental frequency of the binary input signal (hertz)
f_b = input bit rate (bps)
The formula used for modulation index in FM is also valid for FSK; thus,

$$h = \Delta f / f_a \quad \text{(unitless)} \qquad (2.17)$$

where

h = FM modulation index called the h-factor in FSK
f_o = fundamental frequency of the binary modulating signal (hertz)

Δf = peak frequency deviation (hertz)

The peak frequency deviation in FSK is constant and always at its maximum value, and the highest fundamental frequency is equal to half the incoming bit rate. Thus,

$$h = \frac{\frac{|f_m - f_s|}{2}}{\frac{f_b}{2}}$$

or

$$h = \frac{|f_m - f_s|}{f_b} \qquad (2.18)$$

where
h = h-factor (unitless)
f_m = mark frequency (hertz)
f_s = space frequency (hertz)
f_b = bit rate (bits per second)

Example 2-3

Using a Bessel table, determine the minimum bandwidth for the same FSK signal described in Example 2-1 with a mark frequency of 49 kHz, a space frequency of 51 kHz, and an input bit rate of 2 kbps.

Solution The modulation index is found by substituting into Equation 2.17:

$$h = |49 \text{ kHz} - 51 \text{ kHz}| / 2 \text{ kbps} = 1$$
$$= 2 \text{ kHz} / 2 \text{ kbps}$$

From a Bessel table, three sets of significant sidebands are produced for a modulation index of one. Therefore, the bandwidth can be determined as follows:

$$B = 2(3 \times 1000)$$

= 6000 Hz

The bandwidth determined in Example 2-3 using the Bessel table is identical to the bandwidth determined in Example 2-2.

Modulation Index	Carrier	Side Frequency Pairs													
m	J_0	J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}
0.00	1.00	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0.25	0.98	0.12	—	—	—	—	—	—	—	—	—	—	—	—	—
0.5	0.94	0.24	0.03	—	—	—	—	—	—	—	—	—	—	—	—
1.0	0.77	0.44	0.11	0.02	—	—	—	—	—	—	—	—	—	—	—
1.5	0.51	0.56	0.23	0.06	0.01	—	—	—	—	—	—	—	—	—	—
2.0	0.22	0.58	0.35	0.13	0.03	—	—	—	—	—	—	—	—	—	—
2.4	0	0.52	0.43	0.20	0.06	0.02	—	—	—	—	—	—	—	—	—
2.5	−0.05	0.50	0.45	0.22	0.07	0.02	0.01	—	—	—	—	—	—	—	—
3.0	−0.26	0.34	0.49	0.31	0.13	0.04	0.01	—	—	—	—	—	—	—	—
4.0	−0.40	−0.07	0.36	0.43	0.28	0.13	0.05	0.02	—	—	—	—	—	—	—
5.0	−0.18	−0.33	0.05	0.36	0.39	0.26	0.13	0.05	0.02	—	—	—	—	—	—
5.45	0	−0.34	−0.12	0.26	0.40	0.32	0.19	0.09	0.03	0.01	—	—	—	—	—
6.0	0.15	−0.28	−0.24	0.11	0.36	0.36	0.25	0.13	0.06	0.02	—	—	—	—	—
7.0	0.30	0.00	−0.30	−0.17	0.16	0.35	0.34	0.23	0.13	0.06	0.02	—	—	—	—
8.0	0.17	0.23	−0.11	−0.29	−0.10	0.19	0.34	0.32	0.22	0.13	0.06	0.03	—	—	—
8.65	0	0.27	0.06	−0.24	−0.23	0.03	0.26	0.34	0.28	0.18	0.10	0.05	0.02	—	—
9.0	−0.09	0.25	0.14	−0.18	−0.27	−0.06	0.20	0.33	0.31	0.21	0.12	0.06	0.03	0.01	—
10.0	−0.25	0.05	0.25	0.06	−0.22	−0.23	−0.01	0.22	0.32	0.29	0.21	0.12	0.06	0.03	0.01

2-4-2 FSK Transmitter

Figure 2-6 shows a simplified binary FSK modulator, which is very similar to a conventional FM modulator and is very often a voltage-controlled oscillator (VCO).

The center frequency (f_c) is chosen such that it falls halfway between the mark and space frequencies.

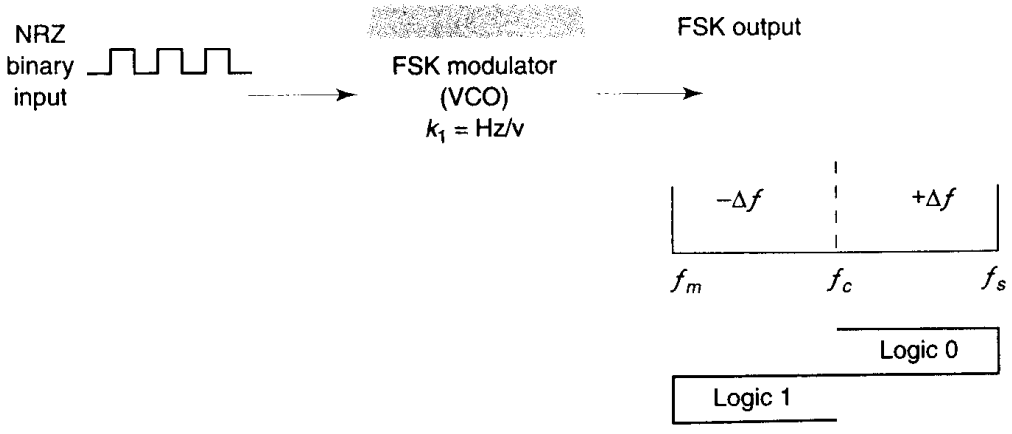


FIGURE 2-6 FSK modulator

A logic 1 input shifts the VCO output to the mark frequency, and a logic 0 input shifts the VCO output to the space frequency.

Consequently, as the binary input signal changes back and forth between logic 1 and logic 0 conditions, the VCO output shifts or deviates back and forth between the mark and space frequencies.

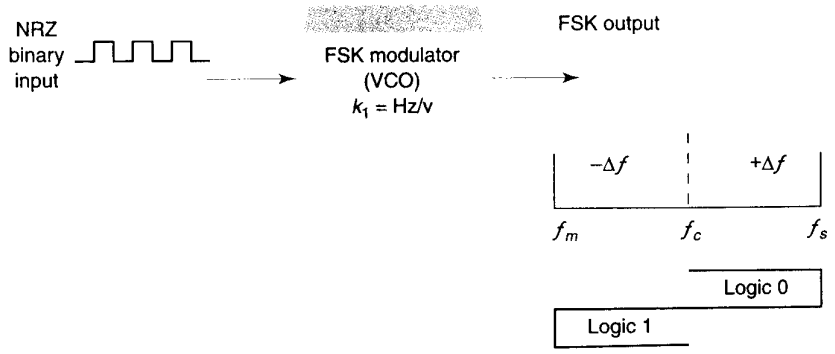


FIGURE 2-6 FSK modulator

A VCO-FSK modulator can be operated in the sweep mode where the peak frequency deviation is simply the product of the binary input voltage and the deviation sensitivity of the VCO.

With the sweep mode of modulation, the frequency deviation is expressed mathematically as

$$\Delta f = v_m(t)k_l \qquad (2\text{-}19)$$

$v_m(t)$ = peak binary modulating-signal voltage (volts)
k_l = deviation sensitivity (hertz per volt).

2-4-3 FSK Receiver

FSK demodulation is quite simple with a circuit such as the one shown in Figure 2-7.

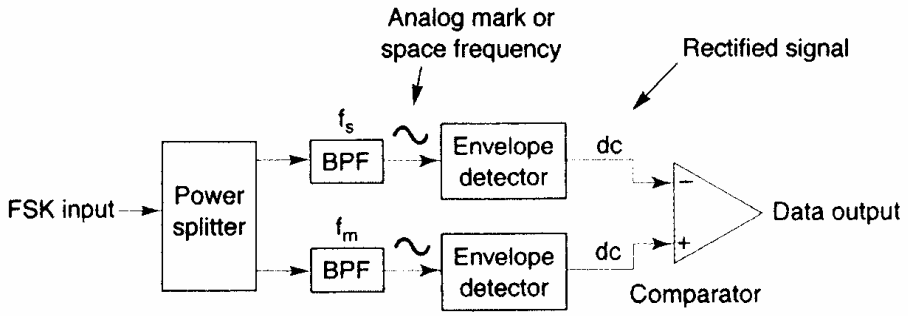


FIGURE 2-7 Noncoherent FSK demodulator

The FSK input signal is simultaneously applied to the inputs of both bandpass filters (BPFs) through a power splitter.

The respective filter passes only the mark or only the space frequency on to its respective envelope detector.

The envelope detectors, in turn, indicate the total power in each passband, and the comparator responds to the largest of the two powers.

This type of FSK detection is referred to as noncoherent detection.

Figure 2-8 shows the block diagram for a coherent FSK receiver.

The incoming FSK signal is multiplied by a recovered carrier signal that has the exact same frequency and phase as the transmitter reference.

However, the two transmitted frequencies (the mark and space frequencies) are not generally continuous; it is not practical to reproduce a local reference that is coherent with both of them. Consequently, coherent FSK detection is seldom used.

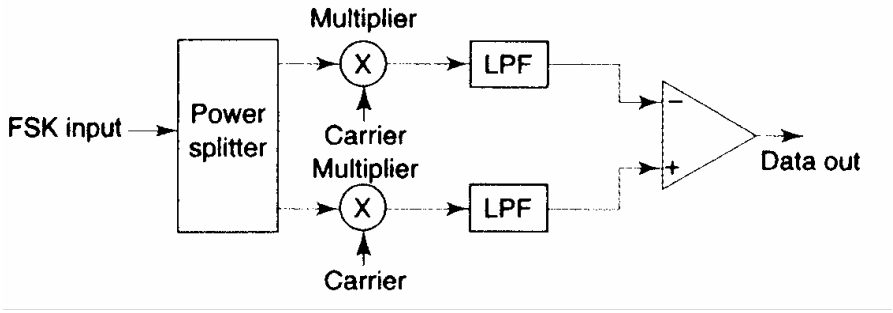


FIGURE 2-8 Coherent FSK demodulator

The most common circuit used for demodulating binary FSK signals is the *phaselocked loop* (PLL), which is shown in block diagram form in Figure 2-9.

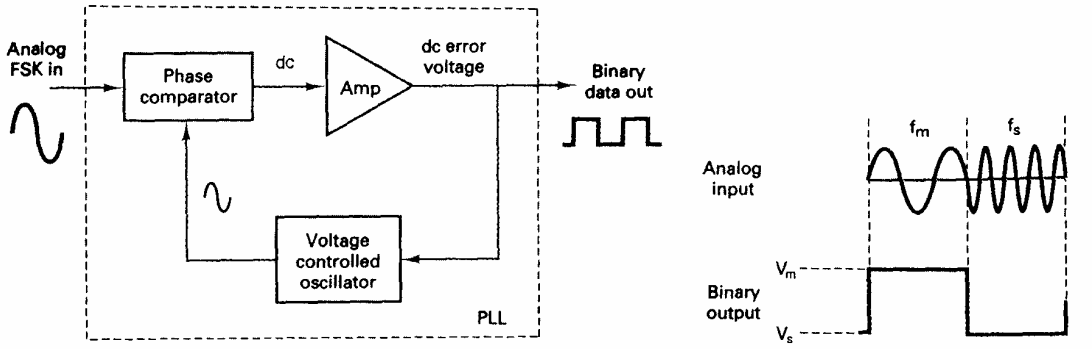


FIGURE 2-9 PLL-FSK demodulator

As the input to the PLL shifts between the mark and space frequencies, the *dc error voltage* at the output of the phase

comparator follows the frequency shift.

Because there are only two input frequencies (mark and space), there are also only two output error voltages. One represents a logic 1 and the other a logic 0.

Binary FSK has a poorer error performance than PSK or QAM and, consequently, is seldom used for high-performance digital radio systems.

Its use is restricted to low-performance, low-cost, asynchronous data modems that are used for data communications over analog, voice-band telephone lines.

2-4-4 Continuous-Phase Frequency-Shift Keying

Continuous-phase frequency-shift keying (CP-FSK) is binary FSK except the mark and space frequencies are synchronized with the input binary bit rate.

With CP-FSK, the mark and space frequencies are selected such that they are separated from the center frequency by an exact multiple of one-half the bit rate (f_m and $f_s = n[f_b / 2]$, where n = any integer).

This ensures a smooth phase transition in the analog output signal when it changes from a mark to a space frequency or vice versa.

Figure 2-10 shows a noncontinuous FSK waveform. It can be seen that when the input changes from a logic 1 to a logic 0 and vice versa, there is an abrupt phase discontinuity in the analog signal. When this occurs, the demodulator has trouble following the frequency shift; consequently, an error may occur.

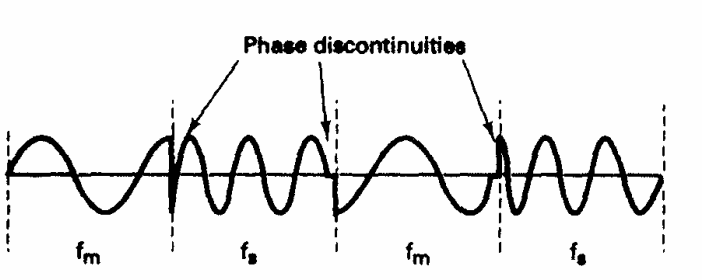


FIGURE 2-10 Noncontinuous FSK waveform

Figure 2-11 shows a continuous phase FSK waveform.

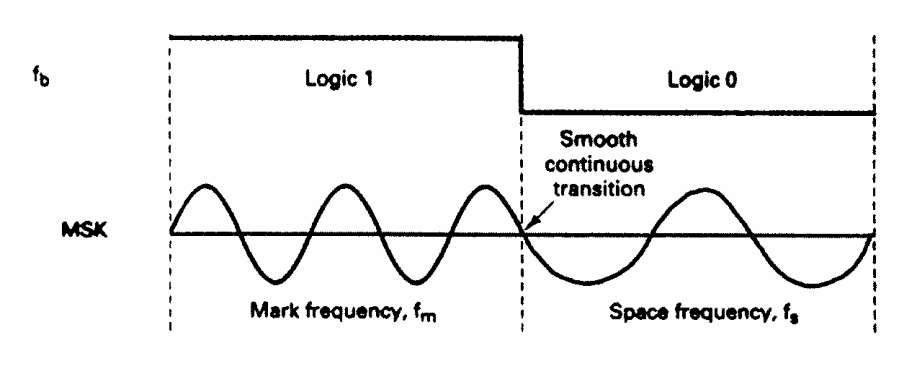


FIGURE 2-11 Continuous-phase MSK waveform

Notice that when the output frequency changes, it is a smooth, continuous transition. Consequently, there are no phase discontinuities.

CP-FSK has a better bit-error performance than conventional binary FSK for a given signal-to-noise ratio.

The disadvantage of CP-FSK is that it requires synchronization circuits and is, therefore, more expensive to implement.

2-5 PHASE-SHIFT KEYING

Phase-shift keying (PSK) is another form of *angle-modulated, constant-amplitude* digital modulation.

2-5-1 Binary Phase-Shift Keying

The simplest form of PSK is *binary phase-shift keying* (BPSK), where N = 1 and *M = 2.*

Therefore, with BPSK, two phases ($2^1 = 2$) are possible for the carrier.

One phase represents a logic 1, and the other phase represents a logic 0. As the input digital signal changes state (i.e., from a 1 to a 0 or from a 0 to a 1), the phase of the output carrier shifts between two angles that are separated by 180°.

Hence, other names for BPSK are *phase reversal keying* (PRK) and *biphase modulation.* BPSK is a form of square-wave modulation of a *continuous wave (CW)* signal.

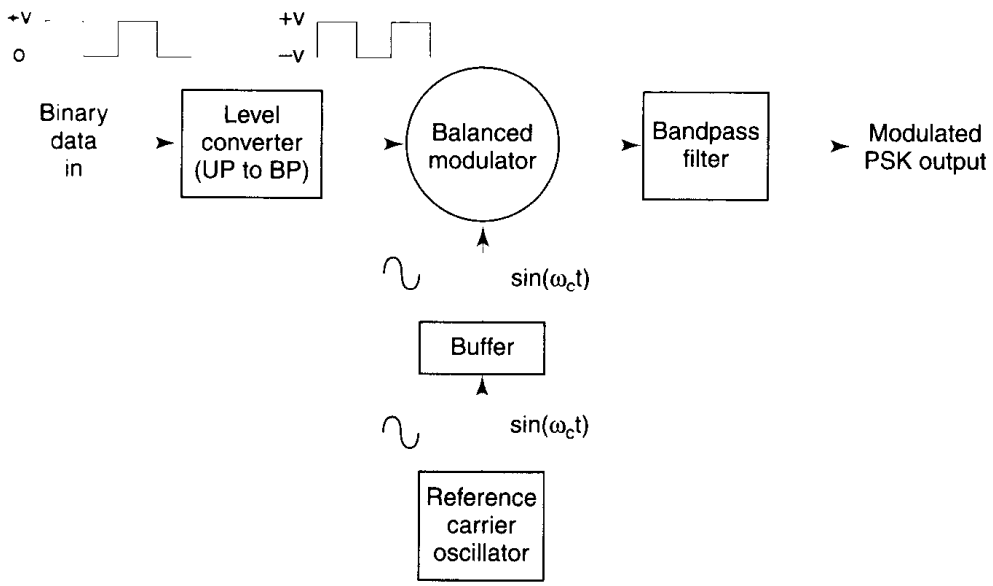


FIGURE 2-12 BPSK transmitter

2-5-1-1 BPSK transmitter.

Figure 2-12 shows a simplified block diagram of a BPSK transmitter.

The balanced modulator acts as a phase reversing switch. Depending on the logic condition of the digital input, the carrier is transferred to the output either in phase or 180° out of phase with the reference carrier oscillator.

Figure 2-13 shows the schematic diagram of a balanced ring modulator.

The balanced modulator has two inputs: a carrier that is in phase with the reference oscillator and the binary digital data.

For the balanced modulator to operate properly, the digital input voltage must be much greater than the peak carrier voltage.

This ensures that the digital input controls the on/off state of diodes D1 to D4. If the binary input is a logic 1(positive voltage), diodes D 1 and D2 are forward biased and on, while diodes D3 and D4 are reverse biased and off (Figure 2-13b). With the polarities shown, the carrier voltage is developed across transformer T2 in phase with the carrier voltage across T 1. Consequently, the output signal is in phase with the reference oscillator.

If the binary input is a logic 0 (negative voltage), diodes Dl and D2 are reverse biased and off, while diodes D3 and D4 are forward biased and on (Figure 9-13c). As a result, the carrier voltage is developed across transformer T2 180° out of phase with the carrier voltage across T 1.

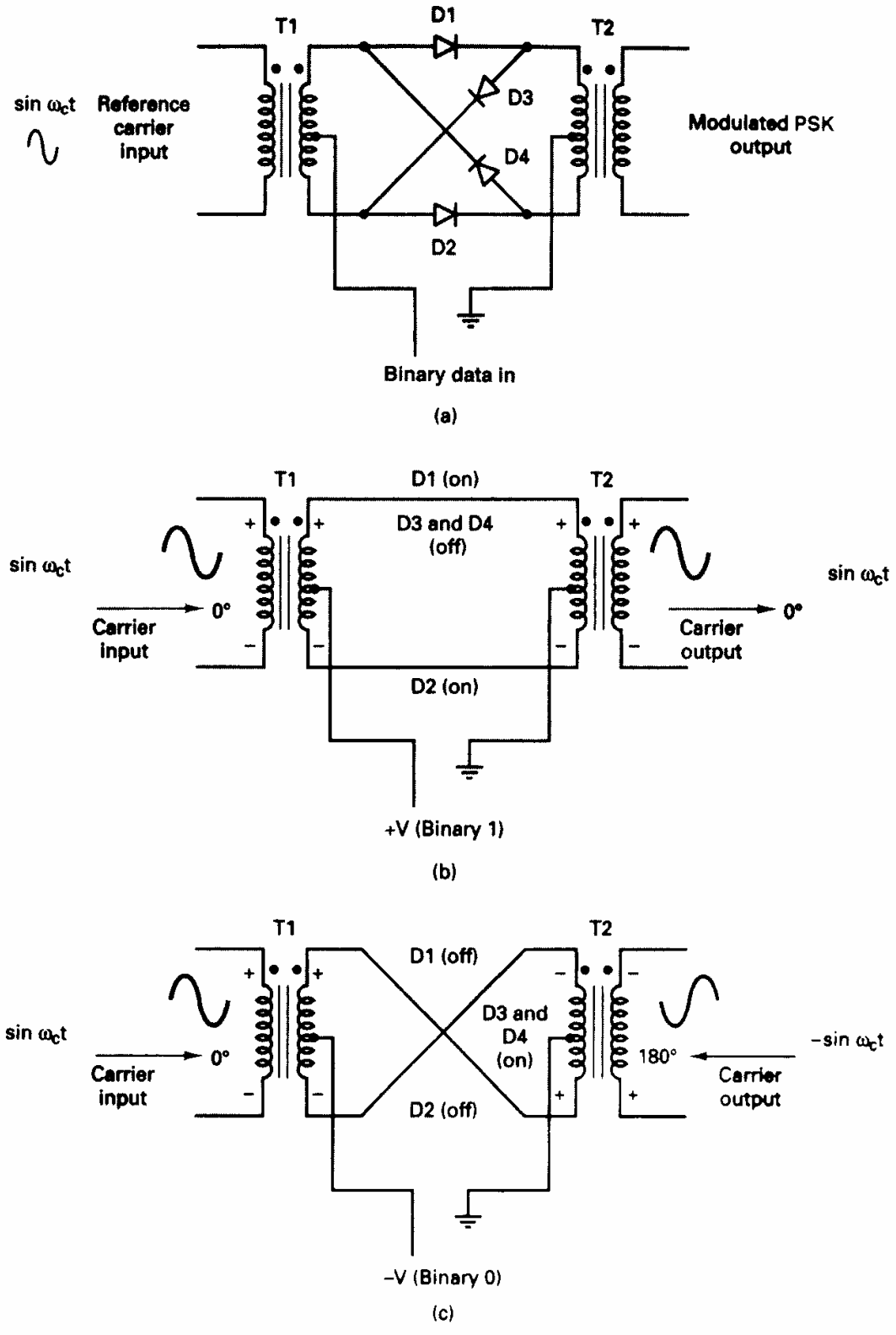


FIGURE 9-13 (a) Balanced ring modulator; (b) logic 1 input; (c) logic 0 input

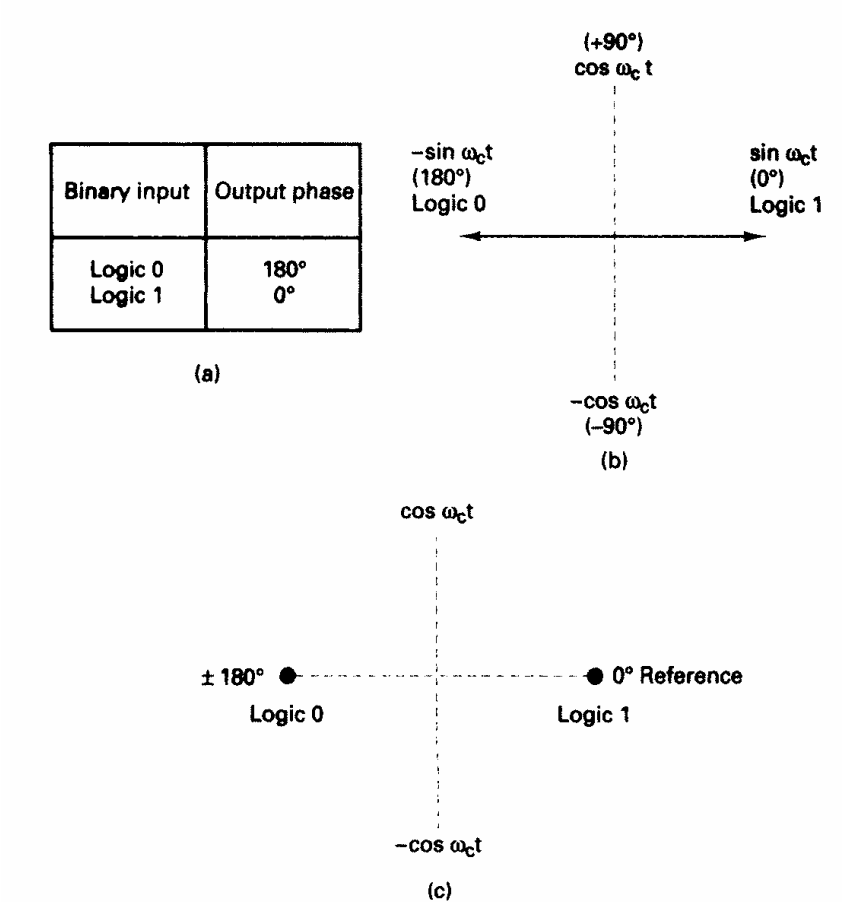


FIGURE 2-14 BPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

2-5-1-2 Bandwidth considerations of BPSK.

In a BPSK modulator. the carrier input signal is multiplied by the binary data.

If + 1 V is assigned to a logic 1 and -1 V is assigned to a logic 0, the input carrier (sin $\omega_c t$) is multiplied by either a + or - 1 .

The output signal is either + 1 sin $\omega_c t$ or -1 sin $\omega_c t$ the first represents a signal that is *in phase* with the reference oscillator, the latter a signal that is 180° out of phase with the reference oscillator.

Each time the input logic condition changes, the output phase changes.

Mathematically, the output of a BPSK modulator is proportional to

$$\text{BPSK output} = [\sin(2\pi f_a t)] \times [\sin(2\pi f_c t)] \qquad (2.20)$$

where
f_a = maximum fundamental frequency of binary input (hertz)
f_c = reference carrier frequency (hertz)

Solving for the trig identity for the product of two sine functions,

$$0.5\cos[2\pi(f_c - f_a)t] - 0.5\cos[2\pi(f_c + f_a)t]$$

Thus, the minimum double-sided Nyquist bandwidth *(B) is*

$$\begin{array}{r} f_c + f_a \\ -(f_c + f_a) \end{array} \qquad \text{or} \qquad \begin{array}{r} f_c + f_a \\ \underline{-f_c + f_a} \\ 2f_a \end{array}$$

and because $f_a = f_b / 2$, where f_b = input bit rate,
where *B is* the minimum double-sided Nyquist bandwidth.

Figure 2-15 shows the output phase-versus-time relationship for a BPSK waveform.

Logic 1 input produces an analog output signal with a 0° phase angle, and a logic 0 input produces an analog output signal with a 180° phase angle.

As the binary input shifts between a logic 1 and a logic 0 condition and vice versa, the phase of the BPSK waveform shifts between 0° and 180°, respectively.

BPSK signaling element (t_s) is equal to the time of one information bit (t_b), which indicates that the bit rate equals the baud.

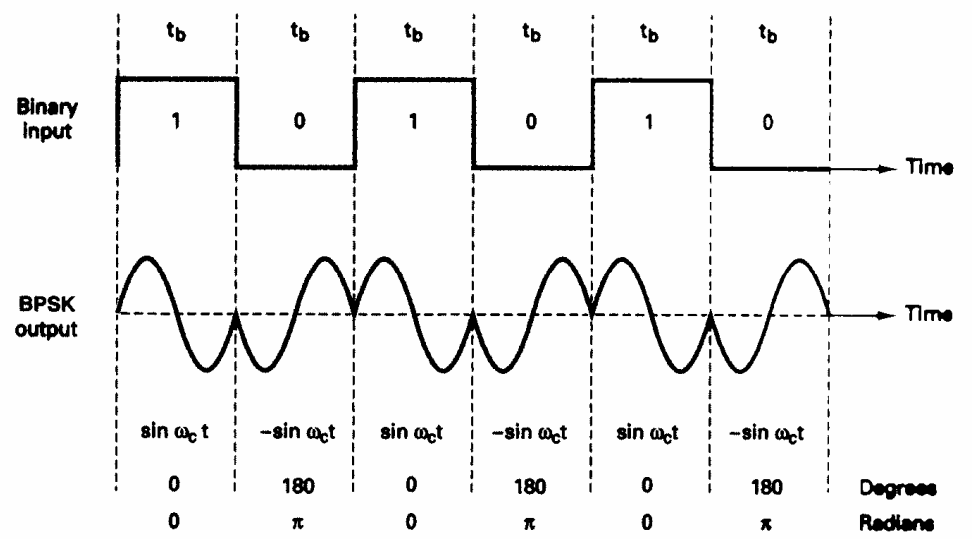


FIGURE 2-15 Output phase-versus-time relationship for a BPSK modulator

Example 2-4

For a BPSK modulator with a carrier frequency of 70 MHz and an input bit rate of 10 Mbps, determine the maximum and minimum upper and lower side frequencies, draw the output spectrum, determine the minimum Nyquist bandwidth, and calculate the baud..

Solution

Substituting into Equation 2-20 yields

output = [sin ($2\pi f_a t$)] x [sin ($2\pi f_c t$)] ; $f_a = f_b / 2 = 5$ MHz

= [sin 2π(5MHz)t)] x [sin 2π(70MHz)t)]

= 0.5cos[2π(70MHz – 5MHz)t] – 0.5cos[2π(70MHz + 5MHz)t]

lower side frequency upper side frequency

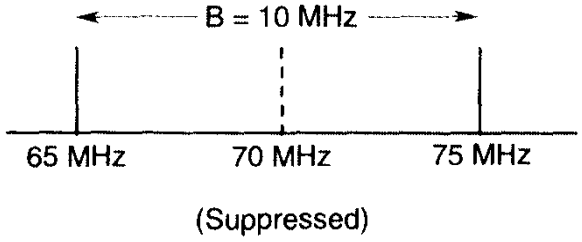
Minimum lower side frequency (LSF):

LSF=70MHz - 5MHz = 65MHz

Maximum upper side frequency (USF):

USF = 70 MHz + 5 MHz = 75 MHz

Therefore, the output spectrum for the worst-case binary input conditions *is* as follows: The minimum Nyquist bandwidth *(B) is*



B = 75 MHz - 65 MHz = 10 MHz

and the baud = f_b or 10 megabaud.

2-5-1-3 BPSK receiver.

Figure 2-16 shows the block diagram of a BPSK receiver.

The input signal maybe $+ \sin \omega_c t$ or $- \sin \omega_c t$.

The coherent carrier recovery circuit detects and regenerates a carrier signal that is both frequency and phase coherent with the original transmit carrier.

The balanced modulator is a product detector; the output is the product d the two inputs (the BPSK signal and the recovered carrier).

The low-pass filter (LPF) operates the recovered binary data from the complex demodulated signal.

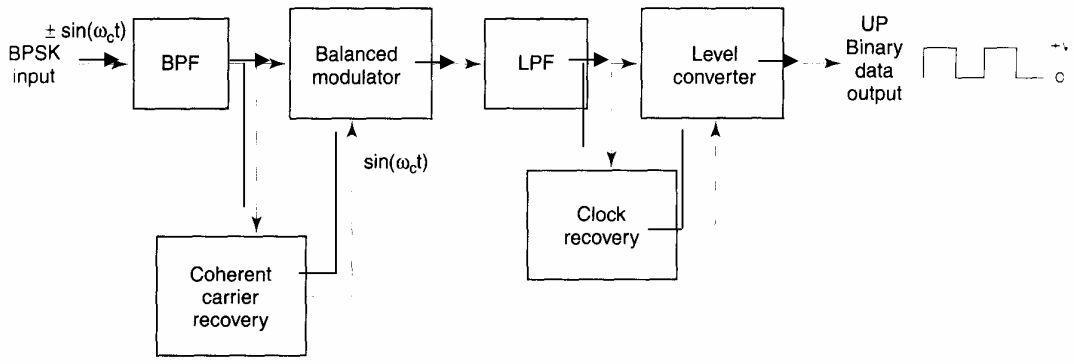


FIGURE 2-16 Block diagram of a BPSK receiver

Mathematically, the demodulation process is as follows.

For a BPSK input signal of + sin $\omega_c t$ (logic 1), the output of the balanced modulator is

$$\text{output} = (\sin \omega_c t)(\sin \omega_c t) = \sin^2 \omega_c t \qquad (2.21)$$

or

$$\sin^2 \omega_c t = 0.5(1 - \cos 2\omega_c t) = 0.5 - 0.5\cos 2\omega_c t$$

filtered out

leaving

$$\text{output} = +0.5 \text{ V} = \text{logic 1}$$

It can be seen that the output of the balanced modulator contains a positive voltage (+[1/2]V) and a cosine wave at twice the carrier frequency (2 $\omega_c t$).

The LPF has a cutoff frequency much lower than 2 $\omega_c t$, and, thus, blocks the second harmonic of the carrier and passes only the positive constant component. A positive voltage represents a demodulated logic 1.

For a BPSK input signal of -sin $\omega_c t$ (logic 0), the output of the balanced modulator is

$$\text{output} = (-\sin \omega_c t)(\sin \omega_c t) = \sin^2 \omega_c t$$

or

$$\sin^2 \omega_c t = -0.5(1 - \cos 2\omega_c t) = 0.5 + 0.5\cos 2\omega_c t$$

filtered out

leaving

output = - 0.5 V = logic 0

The output of the balanced modulator contains a negative voltage (-[l/2]V) and a cosine wave at twice the carrier frequency ($2\omega_c t$).

Again, the LPF blocks the second harmonic of the carrier and passes only the negative constant component. A negative voltage represents a demodulated logic 0.

2-5-2 Quaternary Phase-Shift Keying

QPSK is an M-ary encoding scheme where N = 2 and $M = 4$ (hence, the name "quaternary" meaning "4"). A QPSK modulator is a binary (base 2) signal, to produce four different input combinations,: 00, 01, 10, and 11.

Therefore, with QPSK, the binary input data are combined into groups of two bits, called *dibits.* In the modulator, each dibit code generates one of the four possible output phases (+45°, +135°, -45°, and -135°).

2-5-2-1 QPSK transmitter.

A block diagram of a QPSK modulator is shown in Figure 2-17. Two bits (a dibit) are clocked into the bit splitter. After both bits have been serially inputted, they are simultaneously parallel outputted.

The I bit modulates a carrier that is in phase with the reference oscillator (hence the name "I" for "in phase" channel), and the

Q bit modulate, a carrier that is 90° out of phase.

For a logic 1 = + 1 V and a logic 0= - 1 V, two phases are possible at the output of the I balanced modulator (+sin $\omega_c t$ and - sin $\omega_c t$), and two phases are possible at the output of the Q balanced modulator (+cos $\omega_c t$), and (-cos $\omega_c t$).

When the linear summer combines the two quadrature (90° out of phase) signals, there are four possible resultant phasors given by these expressions: + sin $\omega_c t$ + cos $\omega_c t$, + sin $\omega_c t$ - cos $\omega_c t$, -sin $\omega_c t$ + cos $\omega_c t$, and -sin $\omega_c t$ - cos $\omega_c t$.

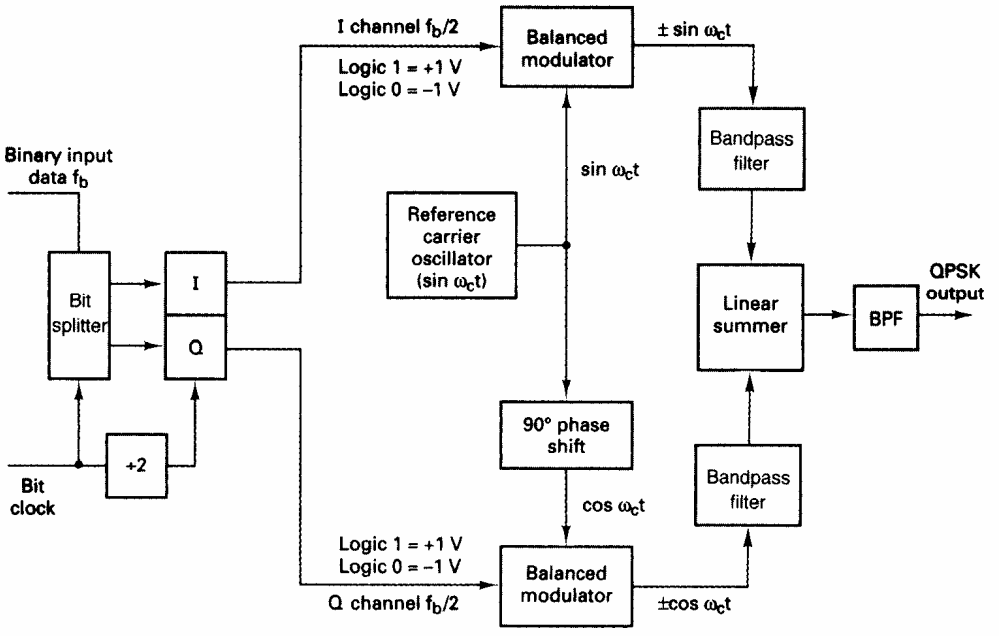


FIGURE 2-17 QPSK modulator

Example 2-5

For the QPSK modulator shown in Figure 2-17, construct the truth table, phasor diagram, and constellation diagram.

Solution

For a binary data input of Q = O and I= 0, the two inputs to the I balanced modulator are -1 and $\sin \omega_c t$, and the two inputs to the Q balanced modulator are -1 and $\cos \omega_c t$.

Consequently, the outputs are

I balanced modulator $=(-1)(\sin \omega_c t) = -1 \sin \omega_c t$
Q balanced modulator $=(-1)(\cos \omega_c t) = -1 \cos \omega_c t$ and the output of the linear summer is

$-1 \cos \omega_c t - 1 \sin \omega_c t = 1.414 \sin(\omega_c t - 135°)$

For the remaining dibit codes (01, 10, and 11), the procedure is the same. The results are shown in Figure 2-18a.

Binary input		QPSK output phase
Q	I	
0	0	−135°
0	1	−45°
1	0	+135°
1	1	+45°

(a)

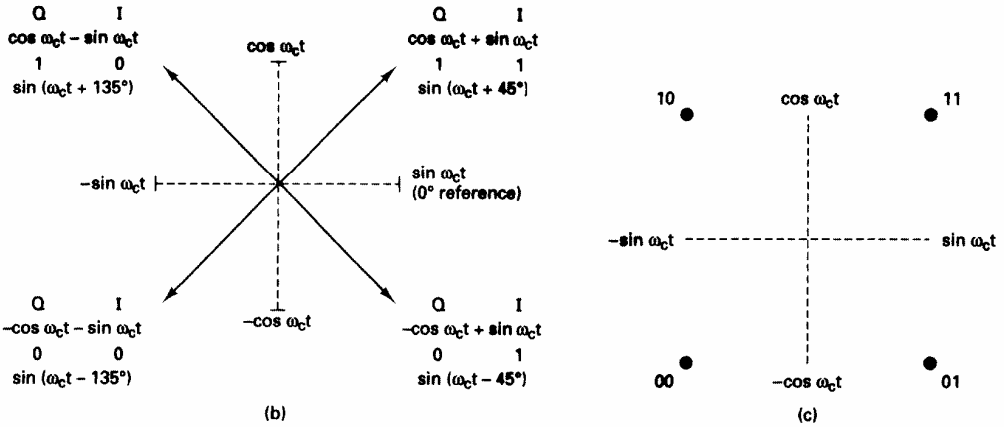


FIGURE 2-18 QPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

In Figures 2-18b and c, it can be seen that with QPSK each of the four possible output phasors has exactly the same amplitude. Therefore, the binary information must be encoded entirely in the phase of the output signal.

Figure 2-18b, it can be seen that the angular separation between any two adjacent phasors in QPSK is 90°.

Therefore, a QPSK signal can undergo almost a+45° or -45° shift in phase during transmission and still retain the correct encoded information when demodulated at the receiver.

Figure 2-19 shows the output phase-versus-time relationship for a QPSK modulator.

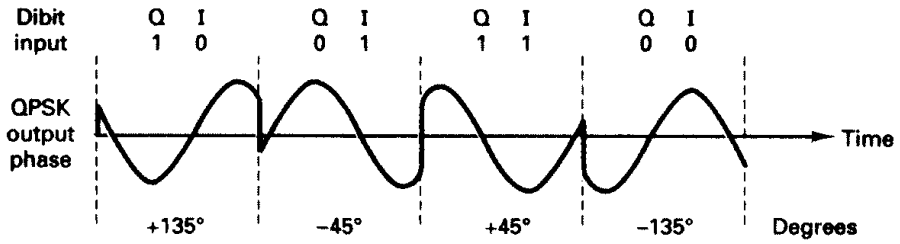


FIGURE 2-19 Output phase-versus-time relationship for a PSK modulator.

2-5-2-2 Bandwidth considerations of QPSK

With QPSK, because the input data are divided into two channels, the bit rate in either the I or the Q channel is equal to one-half of the input data rate ($f_b/2$) (one-half of $f_b/2 = f_b/4$).

This relationship is shown in Figure 2-20.

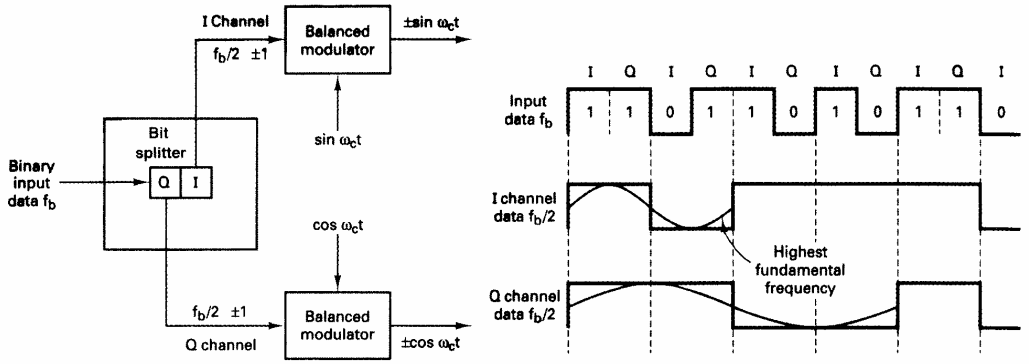


FIGURE 2-20 Bandwidth considerations of a QPSK modulator

In Figure 2-20, it can be seen that the worse-case input condition to the I or Q balanced modulator is an alternative 1/0 pattern, which occurs when the binary input data have a 1100 repetitive pattern. One cycle of the fastest binary transition (a 1/0 sequence in the I or Q channel takes the same time as four input data bits.

Consequently, the highest fundamental frequency at the input and fastest rate of change at the output of the balance.: modulators is equal to one-fourth of the binary input bit rate.

The output of the balanced modulators can be expressed mathematically as

$$\text{output} = (\sin \omega_a t)(\sin \omega_c t) \tag{2.22}$$

where

$$\underbrace{\omega_a t = 2\pi \frac{f_b}{4} t}_{\text{modulating signal}} \quad \text{and} \quad \underbrace{\omega_c t = 2\pi f_c}_{\text{carrier}}$$

$$\text{output} = \left(\sin 2\pi \frac{f_b}{4} t\right)(\sin 2\pi f_c t)$$

$$\frac{1}{2}\cos 2\pi\left(f_c - \frac{f_b}{4}\right)t - \frac{1}{2}\cos 2\pi\left(f_c + \frac{f_b}{4}\right)t$$

The output frequency spectrum extends from $f'_c + f_b / 4$ to $f'_c - f_b / 4$ and the minimum bandwidth (f_N) is

$$\left(f_c + \frac{f_b}{4}\right) - \left(f_c - \frac{f_b}{4}\right) = \frac{2f_b}{4} = \frac{f_b}{2}$$

Example 2-6

For a QPSK modulator with an input data rate (f_b) equal to 10 Mbps and a carrier frequency 70 MHz, determine the minimum double-sided Nyquist bandwidth *(f_N)* and the baud. Also, compare the results with those achieved with the BPSK modulator in

Example 2-4. Use the QPSK block diagram shown in Figure 2-17 as the modulator model.

Solution
The bit rate in both the I and Q channels is equal to one-half of the transmission bit rate, or

$$f_{bQ} = f_{b1} = f_b / 2 = 10 \text{ Mbps} / 2 = 5 \text{ Mbps}$$

The highest fundamental frequency presented to either balanced modulator is

$$f_a = f_{bQ} / 2 = 5 \text{ Mbps} / 2 = 2.5 \text{ MHz}$$

The output wave from each balanced modulator is

$$(\sin 2\pi f_a t)(\sin 2\pi f_c t)$$

$$0.5 \cos 2\pi(f_c - f_a)t - 0.5 \cos 2\pi(f_c + f_a)t$$

$$0.5 \cos 2\pi[(70 - 2.5)\text{MHz}]t - 0.5 \cos 2\pi[(70 - 2.5)\text{MHz}]t$$

$$0.5 \cos 2\pi(67.5\text{MHz})t - 0.5 \cos 2\pi(72.5\text{MHz})t$$

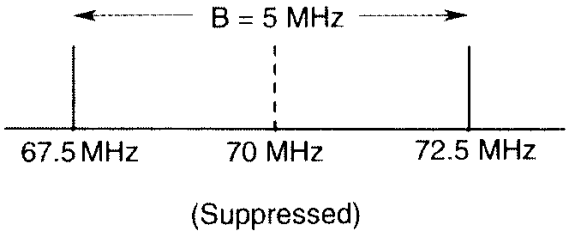
The minimum Nyquist bandwidth is

$$B=(72.5-67.5)\text{MHz} = 5\text{MHz}$$

The symbol rate equals the bandwidth: thus,

symbol rate = 5 megabaud

The output spectrum is as follows:



It can be seen that for the same input bit rate the minimum bandwidth required to pass the output of the QPSK modulator is equal to one-half of that required for the BPSK modulator in Example 2-4. Also, the baud rate for the QPSK modulator is one-half that of the BPSK modulator.

The minimum bandwidth for the QPSK system described in Example 2-6 can also be determined by simply substituting into Equation 2-10:

$$B = 10 \text{ Mbps} / 2 = 5 \text{ MHz}$$

2-5-2-3 (QPSK receiver).

The block diagram of a QPSK receiver is shown in Figure 2-21. The power splitter directs the input QPSK signal to the I and Q product detectors and the carrier recovery circuit. The carrier recovery circuit reproduces the original transmit carrier oscillator signal. The recovered carrier must be frequency and phase coherent with the transmit reference carrier. The QPSK signal is demodulated in the I and Q product detectors, which generate the original I and Q data bits. The outputs of the product detectors are fed to the bit combining circuit, where they are converted from parallel I and Q data channels to a single binary output data stream.

The incoming QPSK signal may be any one of the four possible output phases shown in Figure 2-18. To illustrate the demodulation process, let the incoming QPSK signal be -sin $\omega_c t$ + cos $\omega_c t$. Mathematically, the demodulation process is as follows.

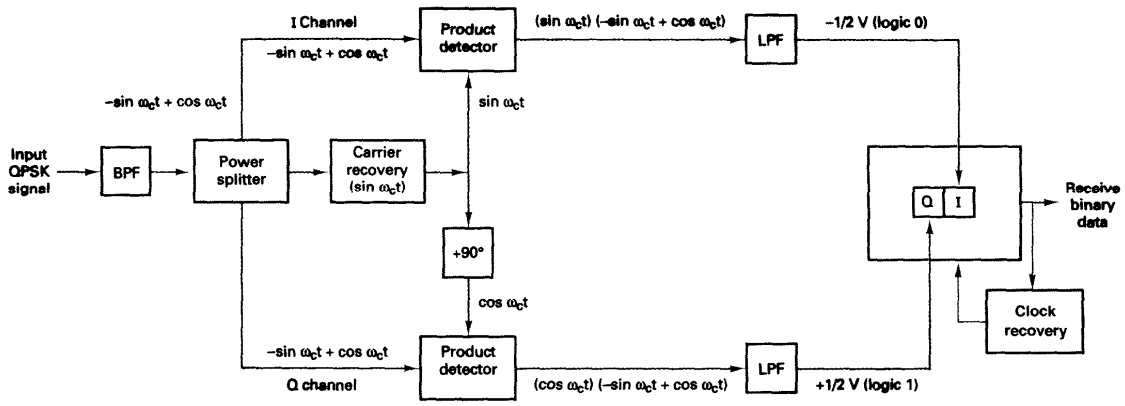


FIGURE 2-21 QPSK receiver

The receive QPSK signal (-sin $\omega_c t$ + cos $\omega_c t$) is one of the inputs to the I product detector. The other input is the recovered carrier (sin $\omega_c t$). The output of the I product detector is

$$\begin{aligned} I &= \underbrace{(-\sin \omega_c t + \cos \omega_c t)}_{\text{QPSK input signal}} \underbrace{(\sin \omega_c t)}_{\text{carrier}} \\ &= (-\sin \omega_c t)(\sin \omega_c t) + (\cos \omega_c t)(\sin \omega_c t) \\ &= -\sin^2 \omega_c t + (\cos \omega_c t)(\sin \omega_c t) \\ &= -\frac{1}{2}(1 - \cos 2\omega_c t) + \frac{1}{2}\sin(\omega_c + \omega_c)t + \frac{1}{2}\sin(\omega_c - \omega_c)t \end{aligned}$$

$$I = -\frac{1}{2} + \frac{1}{2}\cos 2\omega_c t + \frac{1}{2}\sin 2\omega_c t + \frac{1}{2}\sin 0$$

(filtered out) (equals 0)

$$= -\frac{1}{2}\text{V (logic 0)} \qquad (2.23)$$

Again, the receive QPSK signal (-sin $\omega_c t$ + cos $\omega_c t$) is one of the inputs to the Q product detector. The other input is the recovered carrier shifted 90° in phase (cos $\omega_c t$). The output of the Q product detector is

$$
\begin{aligned}
Q &= \underbrace{(-\sin \omega_c t + \cos \omega_c t)}_{\text{QPSK input signal}} \underbrace{(\cos \omega_c t)}_{\text{carrier}} \\
&= \cos^2 \omega_c t - (\sin \omega_c t)(\cos \omega_c t) \\
&= \frac{1}{2}(1 + \cos 2\omega_c t) - \frac{1}{2}\sin(\omega_c + \omega_c)t - \frac{1}{2}\sin(\omega_c - \omega_c)t \\
Q &= \frac{1}{2} + \frac{1}{2}\cos 2\omega_c t - \frac{1}{2}\sin 2\omega_c t - \frac{1}{2}\sin 0 \\
&= \frac{1}{2}\text{V(logic 1)}
\end{aligned}
\qquad (2.24)
$$

(filtered out) (equals 0)

The demodulated I and Q bits (0 and 1, respectively) correspond to the constellation diagram and truth table for the QPSK modulator shown in Figure 2-18.

2-5-2-4 Offset QPSK.

Offset QPSK (OQPSK) is a modified form of QPSK where the bit waveforms on the I and Q channels are offset or shifted in phase from each other by one-half of a bit time.

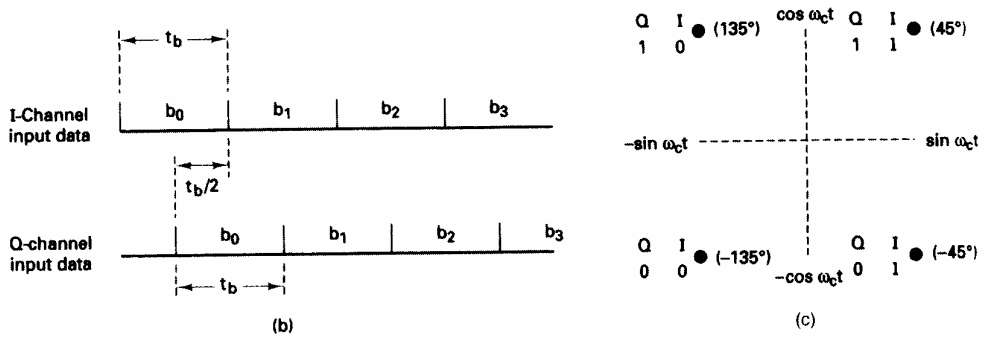


FIGURE 2-22 Offset keyed (OQPSK): (a) block diagram; (b) bit alignment; (c) constellation diagram

Because changes in the I channel occur at the midpoints of the Q channel bits and vice versa, there is never more than a single bit change in the dibit code and, therefore, there is never more than a 90° shift in the output phase. In conventional QPSK, a change in the input dibit from 00 to 11 or 01 to 10 causes a corresponding 180° shift in the output phase.

Therefore, an advantage of OQPSK is the limited phase shift that must be imparted during modulation.

A disadvantage of OQPSK is that changes in the output phase occur at twice the data rate in either the I or Q channel".

Consequently, with OQPSK the baud and minimum bandwidth are twice that of conventional QPSK for a given transmission bit rate. OQPSK is sometimes called OKQPSK *(offset-keyed QPSK).*

2-5-3 8-PSK

With *8-PSK,* three bits are encoded, forming tribits and producing eight different output phases. To encode eight different phases, the incoming bits are encoded in groups of three, called tribits ($2^3 = 8$).

2-5-3-1 8-PSK transmitter.

A block diagram of an 8-PSK modulator is shown in Figure 2-23.

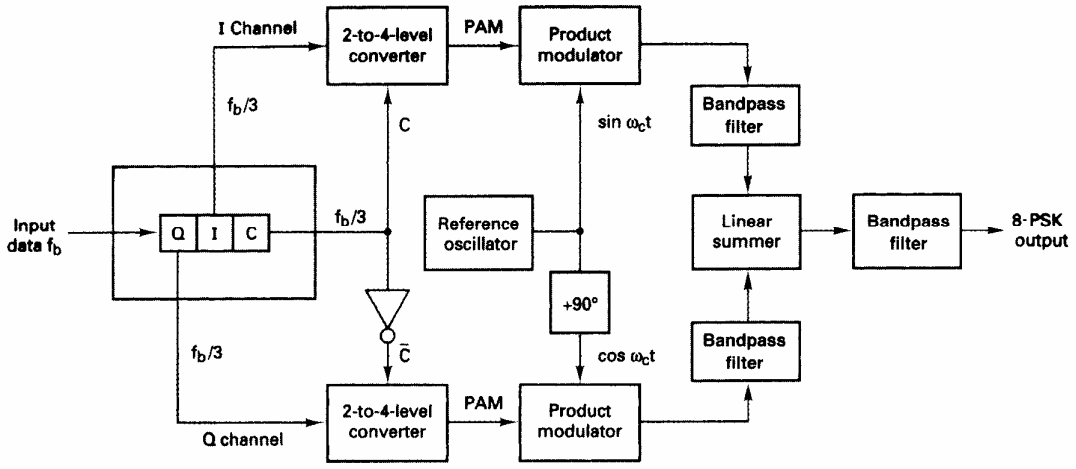
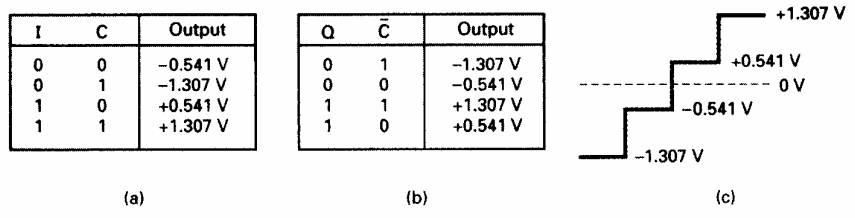


FIGURE 2.23 8-PSK modulator



I	C	Output
0	0	−0.541 V
0	1	−1.307 V
1	0	+0.541 V
1	1	+1.307 V

(a)

Q	$\bar{C}$	Output
0	1	−1.307 V
0	0	−0.541 V
1	1	+1.307 V
1	0	+0.541 V

(b)

(c)

FIGURE 2-24 I- and Q-channel 2-to-4-level converters: (a) 1-channel truth table; (b) D-channel truth table; (c) PAM levels

The bit rate in each of the three channels is f_b,/3.

The bits in the I and C channels enter the I channel 2-to-4-level converter and the bits in the Q and C channels enter the Q channel 2-to-4-level converter.

Essentially, the 2-to-4-level converters are parallel-input *digital-to-analog converter* (DACs). With two input bits, four output voltages are possible.

The I or Q bit determines the polarity of the output analog signal (logic 1=+V and logic 0 = -V), whereas the C or C bit determines the magnitude (logic 1= 1.307 V and logic 0 = 0.541 V).

Figure 2-24 shows the truth table and corresponding output conditions for the 2-to4-level converters. Because the C and $\bar{C}$ bits can never be the same logic state, the outputs from the I and Q 2-to-4-level converters can never have the same magnitude, although they can have the same polarity. The output of a 2-to-4-level converter is an M-ary, *pulse-amplitude-modulated* (PAM) signal where M = 4.

Example 2-7

For a tribit input of Q = 0, 1 = 0, and C = 0 (000), determine the output phase for the S-PSK modulator shown in Figure 2-23.

Solution

The inputs to the I channel 2-to-4-level converter are I = 0 and C = 0. From Figure 2-24 the output is -0.541 V. The inputs to the Q channel 2-to-4-level converter are Q = 0 and $\bar{C}$ = 1.

Again from Figure 2-24, the output is - 1.307 V.

Thus, the two inputs to the I channel product modulators are -0.541

and sin $\omega_c t$. The output is

$$I = (-0.541)(\sin \omega_c t) = -0.541 \sin \omega_c t$$

The two inputs to the Q channel product modulator are - 1.307 V and cos $\omega_c t$. The output is

$$Q = (-1.307)(\cos \omega_c t) = -1.307 \cos \omega_c t$$

The outputs of the I and Q channel product modulators are combined in the linear summer and produce a modulated output of

$$\text{summer output} = -0.541 \sin \omega_c t - 1.307 \cos \omega_c t$$

$$= 1.41 \sin(\omega_c t - 112.5°)$$

For the remaining tribit codes (001, 010, 011, 100, 101, 110, and 111), the procedure is the same. The results are shown in Figure 2-25.

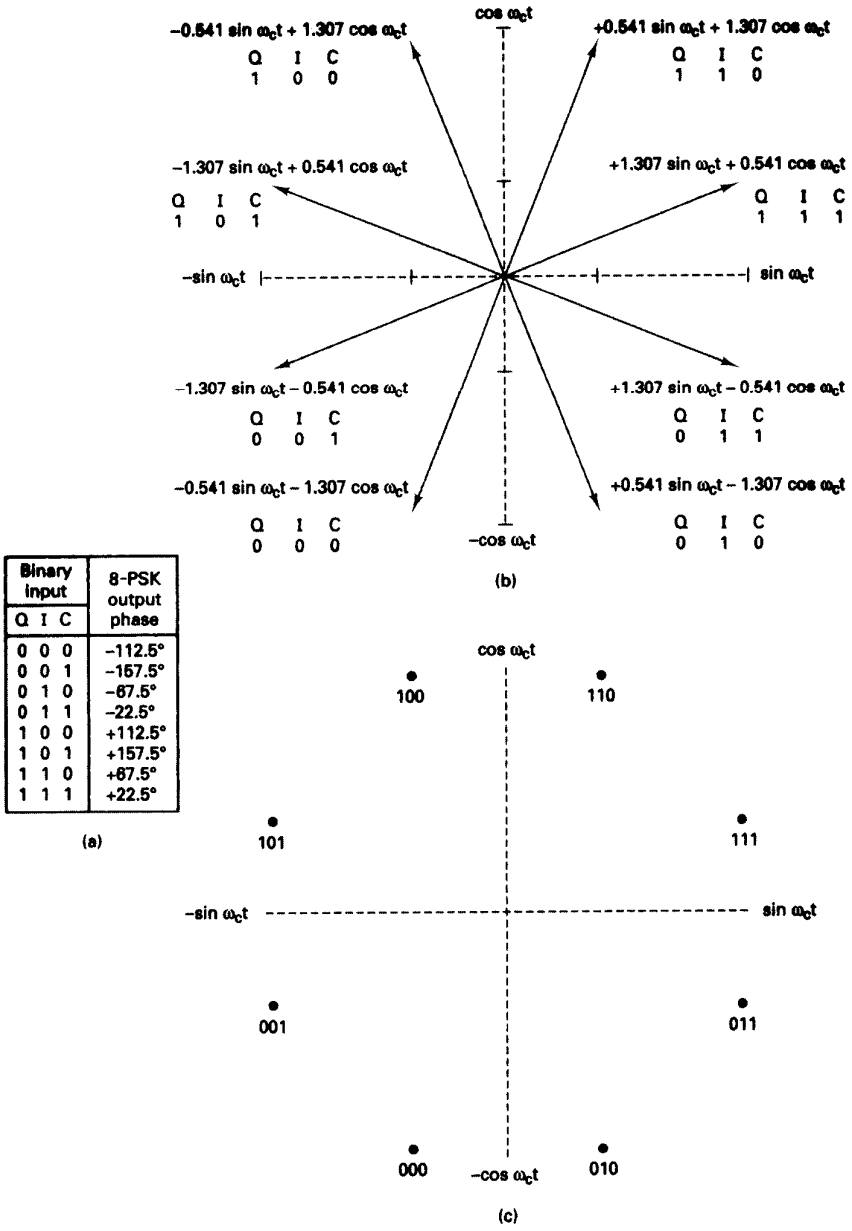


FIGURE 2-25 8-PSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram.

From Figure 2-25, it can be seen that the angular separation between any two adjacent phasors is 45°, half what it is with QPSK.

Therefore, an 8-PSK signal can undergo almost a ± 22.5° phase shift during transmission and still retain its integrity. Also, each phasor is of equal magnitude; the tribit condition (actual information) is again contained only in the phase of the signal.

The PAM levels of 1.307 and 0.541 are relative values. Any levels may be used as long as their ratio is 0.541/1.307 and their arc tangent is equal to 22.5°. For example, if their values were doubled to 2.614 and 1.082, the resulting phase angles would not change, although the magnitude of the phasor would increase proportionally.

Figure 2-26 shows the output phase-versus-time relationship of an 8-PSK modulator.

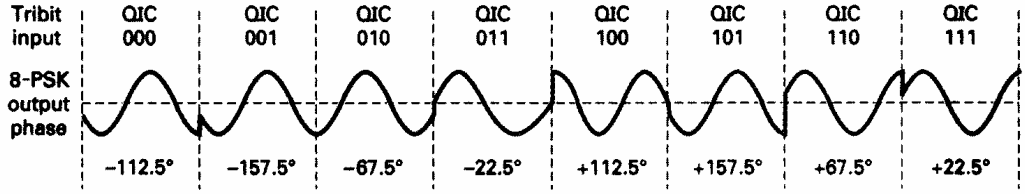


FIGURE 2-26 Output phase-versus-time relationship for an 8-PSK modulator

2-5-3-2 Bandwidth considerations of 8-PSK.

With 8-PSK, because the data are divided into three channels, the bit rate in the I, Q, or C channel is equal to one-third of the binary input data rate *(f_b/3).*

$$\theta = (X \sin \omega_a t)(\sin \omega_c t) \tag{2.25}$$

where

$$\underbrace{\omega_a t = 2\pi \frac{f_b}{6} t}_{\text{modulating signal}} \quad \text{and} \quad \underbrace{\omega_c t = 2\pi f_c t}_{\text{carrier}}$$

And $X = \pm 1.307$ or ± 0.541

Thus

$$\theta = \left(X \sin 2\pi \frac{f_b}{6} t\right)(\sin 2\pi f_c t)$$

$$= \frac{X}{2} \cos 2\pi \left(f_c - \frac{f_b}{6}\right) t - \frac{X}{2} \cos 2\pi \left(f_c + \frac{f_b}{6}\right) t$$

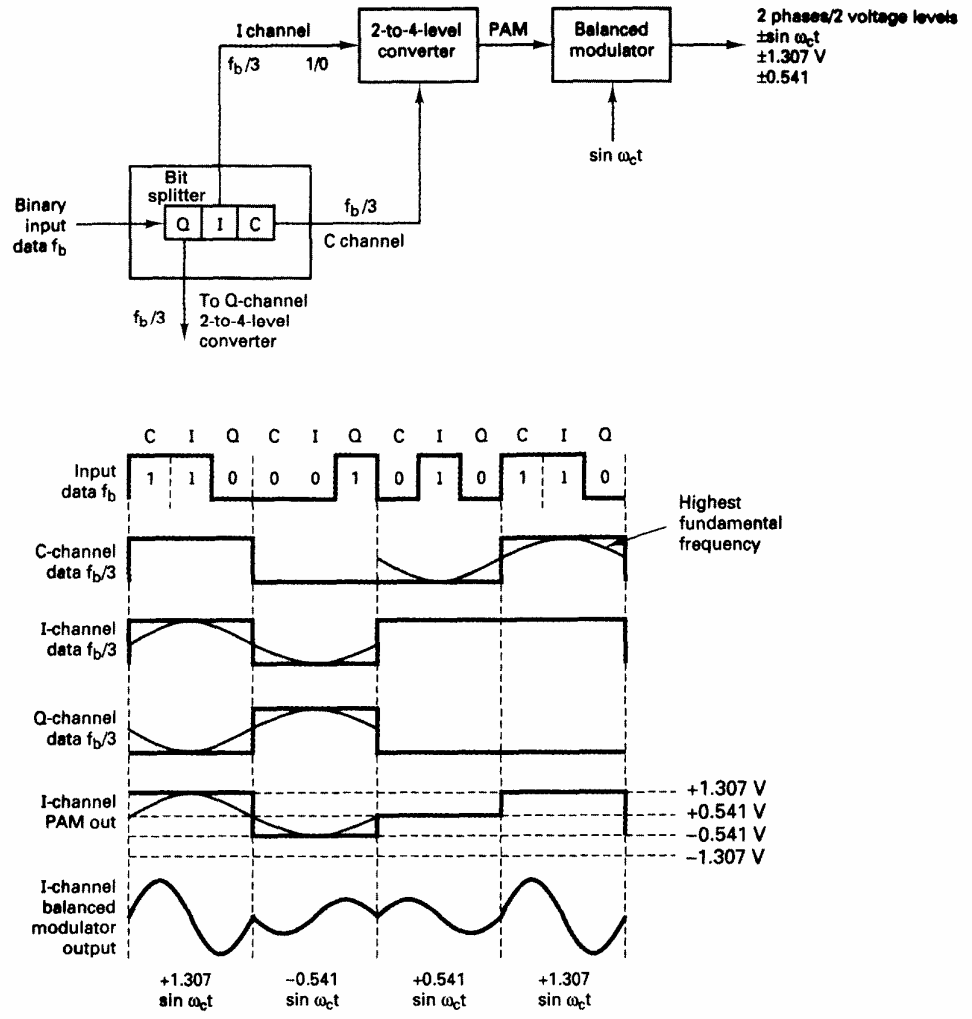


FIGURE 2-27 Bandwidth considerations of an 8-PSK modulator

Figure 2-27 shows that the highest fundamental frequency in the I, Q, or C channel is equal to one-sixth the bit rate of the binary input (one cycle in the I, Q, or C channel takes the same amount of time as six input bits).

With an 8-PSK modulator, there is one change in phase at the output for every three data input bits. Consequently, the baud for 8 PSK equals $f_b / 3$, the same as the minimum bandwidth. Again, the balanced modulators are product modulators; their outputs are the product of the carrier and the PAM signal.

Mathematically, the output of the balanced modulators is

The output frequency spectrum extends from $f_c + f_b/6$ to $f_c - f_b/6$, and the minimum bandwidth (f_N) is

$$\left(f_c + \frac{f_b}{6}\right) - \left(f_c - \frac{f_b}{6}\right) = \frac{2f_b}{6} = \frac{f_b}{3}$$

Example 2-8

For an 8-PSK modulator with an input data rate *(fb)* equal to 10 Mbps and a carrier frequency of 70 MHz, determine the minimum double-sided Nyquist bandwidth (f_N) and the baud. Also, compare the results with those achieved with the BPSK and QPSK modulators in Examples 2-4 and 2-6. If the 8-PSK block diagram shown in Figure 2-23 as the modulator model.

Solution

The bit rate in the I, Q, and C channels is equal to one-third of the input bit rate, or 10 Mbps

$$f_{bc} = f_{bQ} = f_{b1} = 10 \text{ Mbps} / 3 = 3.33 \text{ Mbps}$$

Therefore, the fastest rate of change and highest fundamental frequency presented to either balanced modulator is

$$f_a = f_{bc} / 2 = 3.33 \text{ Mbps} / 2 = 1.667 \text{ Mbps}$$

The output wave from the balance modulators is

$$(\sin 2\pi f_a t)(\sin 2\pi f_c t)$$

$$0.5 \cos 2\pi(f_c - f_a)t - 0.5 \cos 2\pi(f_c + f_a)t$$

$$0.5 \cos 2\pi[(70 - 1.667)\text{MHz}]t - 0.5 \cos 2\pi[(70$$

+ 1.667)MHz]t

$$0.5 \cos 2\pi(68.333\text{MHz})t - 0.5 \cos 2\pi(71.667\text{MHz})t$$

The minimum Nyquist bandwidth is

$$B = (71.667 - 68.333)\ \text{MHz} = 3.333\ \text{MHz}$$

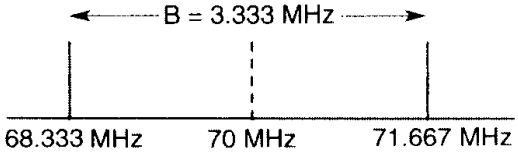
The minimum bandwidth for the 8-PSK can also be determined by simply substituting into Equation 2-10:

$$B = 10\ \text{Mbps} / 3 = 3.33\ \text{MHz}$$

Again, the baud equals the bandwidth; thus,

baud = 3.333 megabaud

The output spectrum is as follows:



B = 3.333 MHz

It can be seen that for the same input bit rate the minimum bandwidth required to pass the output of an 8-PSK modulator is equal to one-third that of the BPSK modulator in Example 2-4 and 50% less than that required for the QPSK modulator in Example 2-6. Also, in each case the baud has been reduced by the same proportions.

2-5-3-3 8-PSK receiver.

Figure 2-28 shows a block diagram of an 8-PSK receiver. The power splitter directs the input 8-PSK signal to the I and Q product detectors and the carrier recovery circuit.

The carrier recovery circuit reproduces the original reference oscillator signal. The incoming 8-PSK signal is mixed with the recovered carrier in the I product detector and with a quadrature carrier in the Q product detector.

The outputs of the product detectors are 4-level PAM signals that are fed to the 4-to-2-level *analog-to-digital converters* (ADCs). The outputs from the I channel 4-to-2-level converter are the I and C bits, whereas the outputs from the Q channel 4-to-2-level converter are the Q and $\bar{C}$ bits. The parallel-to-serial logic circuit converts the I/C and Q/$\bar{C}$ bit pairs to serial I, Q, and C output data streams.

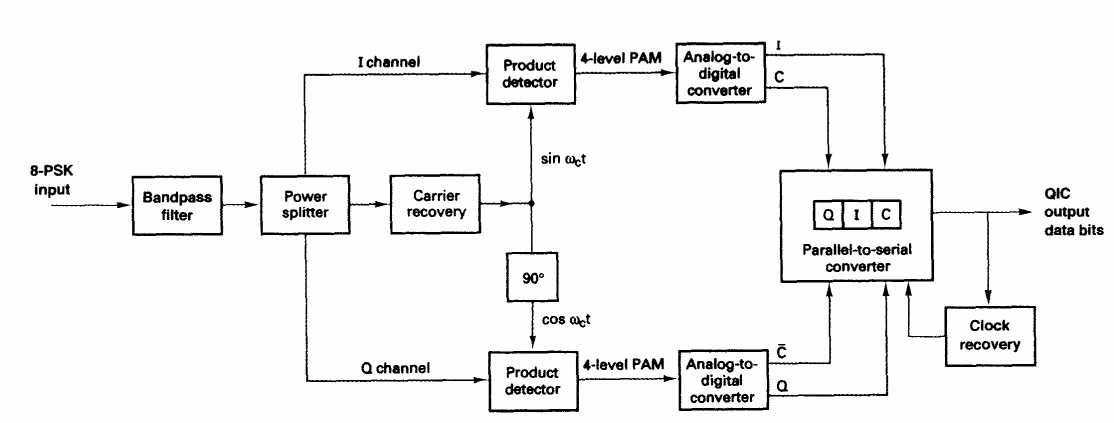


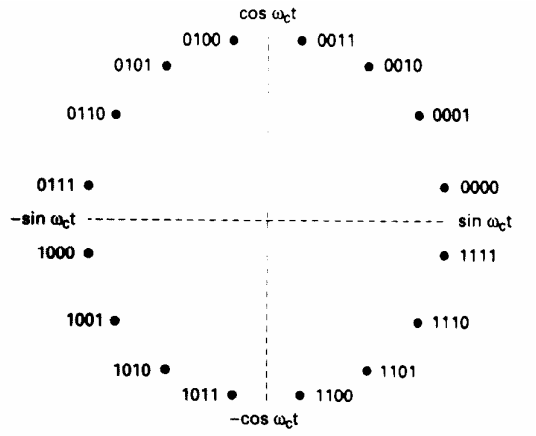
FIGURE 2-28 8-PSK receiver.

2-5-4 16-PSK

16-PSK is an M-ary encoding technique where M = 16; there are 16 different output phases possible. With 16-PSK, four bits (called *quadbits)* are combined, producing 16 different output phases. With 16-PSK, n = 4 and M = 16; therefore, the minimum bandwidth and baud equal one-fourth the bit rate ($f_b/4$).

Bit code	Phase	Bit code	Phase
0000	11.25°	1000	191.25°
0001	33.75°	1001	213.75°
0010	56.25°	1010	236.25°
0011	78.75°	1011	258.75°
0100	101.25°	1100	281.25°
0101	123.75°	1101	303.75°
0110	146.25°	1110	326.25°
0111	168.75°	1111	348.75°

(a)



(b)

FIGURE 2-29 16-PSK: (a) truth table; (b) constellation diagram

Figure 2-29 shows the truth table and constellation diagram for 16-PSK, respectively. Comparing Figures 2-18, 2-25, and 2-29 shows that as the level of encoding increases (i.e., the values of n and M increase), more output phases are possible and the closer each point on the constellation diagram is to an adjacent point. With 16-PSK, the angular separation between adjacent output phases is only 22.5° (180^0 / 8). Therefore, 16-PSK can undergo only a 11.25° (180^0 / 16) phase shift during transmission and still retain its integrity.

For an M-ary PSK system with 64 output phases (n = 6), the angular separation between adjacent phases is only 5.6° (180 / 32). This is an obvious limitation in the level of encoding (and

bit rates) possible with PSK, as a point is eventually reached where receivers cannot discern the phase of the received signaling element. In addition, phase impairments inherent on communications lines have a tendency to shift the phase of the PSK signal, destroying its integrity and producing errors.

2.6 QUADRATURE – AMPLITUDE MODULATION

2-6-1 8-QAM

8-QAM is an M-ary encoding technique where M = 8. Unlike 8-PSK, the output signal from an 8-QAM modulator is not a constant-amplitude signal.

2-6-1-1 8-QAM transmitter.

Figure 2-30a shows the block diagram of an 8-QAM transmitter. As you can see, the only difference between the 8-QAM transmitter and the 8PSK transmitter shown in Figure 2-23 is the omission of the inverter between the C channel and the Q product modulator. As with 8-PSK, the incoming data are divided into groups of three bits (tribits): the I, Q, and C bit streams, each with a bit rate equal to one-third of the incoming data rate. Again, the I and Q bits determine the polarity of the PAM signal at the output of the 2-to-4-level converters, and the C channel determines the magnitude. Because the C bit is fed uninverted to both the I and the Q channel 2-to-4-level converters. the magnitudes of the I and Q PAM signals are always equal. Their polarities depend on the logic condition of the I and Q bits and, therefore, may be different. Figure 2-30b shows the truth table for the I and Q channel 2-to-4-level converters; they are identical.

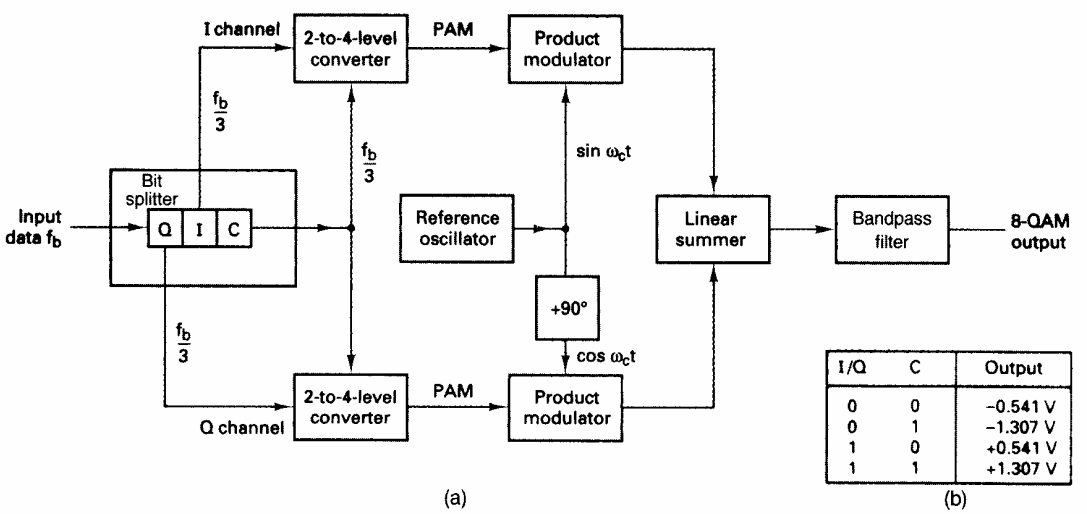


FIGURE 2-30 8-OAM transmitter: (a) block diagram; (b) truth table 2-4 level converters

Example 2-9

For a tribit input of Q = 0, I= 0, and C = 0 (000), determine the output amplitude and phase for the 8-QAM transmitter shown in Figure 2-30a.

Solution

The inputs to the I channel 2-to-4-level converter are I= 0 and C = 0. From Figure 2-30b,
the output is -0.541 V. The inputs to the Q channel 2-to-4-level converter are Q = 0 and C = 0. Again from Figure 9-30b, the output is -0.541 V.

Thus, the two inputs to the I channel product modulator are -0.541 and sin $\omega_c t$. The output is

$$I = (-0.541)(\sin \omega_c t) = -0.541 \sin \omega_c t.$$

The two inputs to the Q channel product modulator are -0.541 and cos $\omega_c t$.. The output is

$$Q = (-0.541)(\cos \omega_c t.) = -0.541 \cos \omega_c t.$$

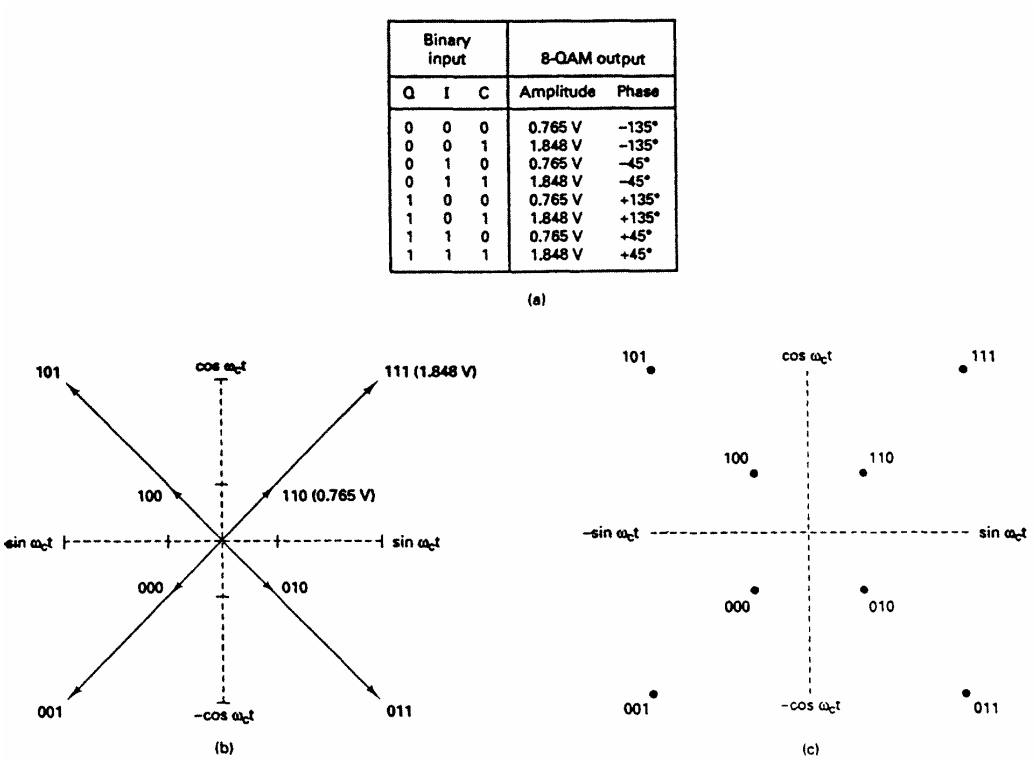
The outputs from the I and Q channel product modulators are combined in the linear summer and produce a modulated output of

$$\text{summer output} = -0.541 \sin \omega_c t. - 0.541 \cos \omega_c t.$$

$$= 0.765 \sin(\cos - 135°)$$

For the remaining tribit codes (001, 010, 0ll, 100, 101, 110, and 111), the procedure is the same. The results are shown in Figure 2-31.

Figure 2-32 shows the output phase-versus-time relationship for an 8-QAM modulator. Note that there are two output amplitudes, and only four phases are possible.



Binary input			8-QAM output	
Q	I	C	Amplitude	Phase
0	0	0	0.765 V	−135°
0	0	1	1.848 V	−135°
0	1	0	0.765 V	−45°
0	1	1	1.848 V	−45°
1	0	0	0.765 V	+135°
1	0	1	1.848 V	+135°
1	1	0	0.765 V	+45°
1	1	1	1.848 V	+45°

(a)

FIGURE 2-31 8-QAM modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

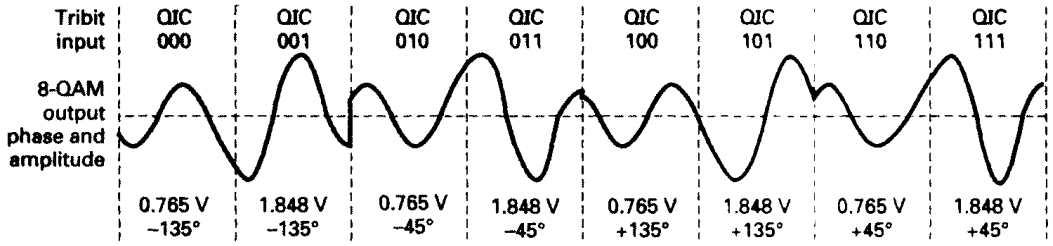


FIGURE 2-32 Output phase and amplitude-versus-time relationship for 8-QAM

2-6-1-2 Bandwidth considerations of 8-QAM.

The minimum bandwidth required for 8-QAM is f_b / *3,* the same as in 8-PSK.

2-6-1-3 8-QAM receiver.

An 8-QAM receiver is almost identical to the 8-PSK receiver shown in Figure 2-28.

2-6-2 16-QAM

As with the 16-PSK, *16-QAM* is an M-ary system where M = 16. The input data are acted on in groups of four (2^4 = 16). As with 8-QAM, both the phase and the amplitude of the transmit carrier are varied.

2-6-2-1 QAM transmitter.

The block diagram for a 16-QAM transmitter is shown in Figure 2-33.

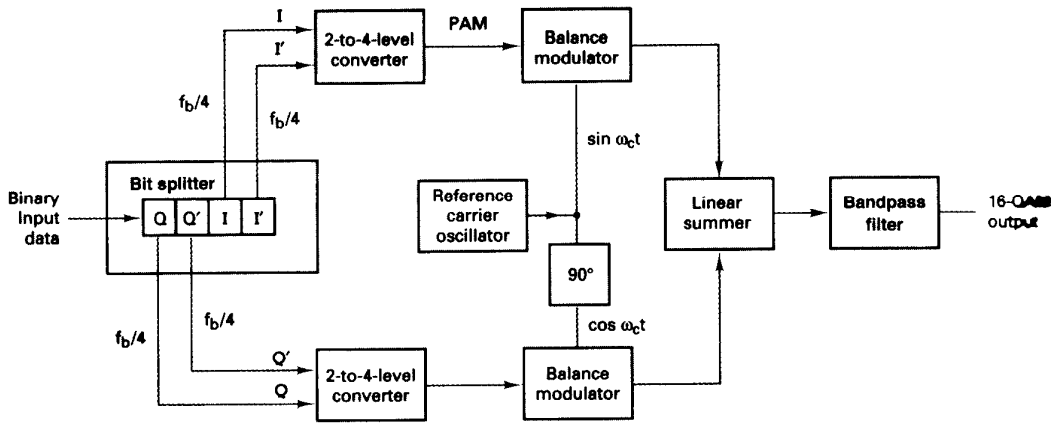


FIGURE 2-33 16-QAM transmitter block diagram

The input binary data are divided into four channels: I, I', Q, and Q'. The bit rate in each channel is equal to one-fourth of the input bit rate ($f_b/4$).

The I and Q bits determine the polarity at the output of the 2-to-4-level converters (a logic 1 = positive and a logic 0 = negative).

The I' and Q' buy determine the magnitude (a logic 1 = 0.821 V and a logic 0 = 0.22 V).

For the I product modulator they are +0.821 sin $\omega_c t$, -0.821 sin $\omega_c t$, +0.22 sin $\omega_c t$, and -0.22 sin $\omega_c t$.

For the Q product modulator, they are +0.821 cos $\omega_c t$, +0.22 cos $\omega_c t$, -0.821 cos $\omega_c t$, and -0.22 cos $\omega_c t$.

The linear summer combines the outputs from the I and Q channel product modulators and produces the 16 output conditions necessary for 16-QAM. Figure 2-34 shows the truth table for the I and Q channel 2-to-4-level converters.

I	I'	Output
0	0	−0.22 V
0	1	−0.821 V
1	0	+0.22 V
1	1	+0.821 V

(a)

Q	Q'	Output
0	0	−0.22 V
0	1	−0.821 V
1	0	+0.22 V
1	1	+0.821 V

(b)

FIGURE 2-34 Truth tables for the I- and Q-channel 2-to-4-evel converters: (a) I channel; (b) Q channel

Example 2-10

For a quadbit input of I= 0, I' = 0, Q = 0, and Q' = 0 (0000), determine the output amplitude and phase for the 16-QAM modulator shown in Figure 2-33.

Solution

The inputs to the I channel 2-to-4-level converter are I = 0 and I' = 0. From Figure 2-34, the output is -0.22 V. The inputs to the Q channel 2-to-4-level converter are Q= 0 and Q' = 0. Again from Figure 2-34, the output is -0.22 V.

Thus, the two inputs to the I channel product modulator are -0,22 V and sin $\omega_c t$. The output is

$$I = (-0.22)(\sin \omega_c t) = -0.22 \sin \omega_c t$$

The two inputs to the Q channel product modulator are -0.22 V and cos $\omega_c t$. The output is

$$Q = (-0.22)(\cos \omega_c t) = -0.22 \cos \omega_c t$$

The outputs from the I and Q channel product modulators are combined in the linear summer and produce a modulated output of

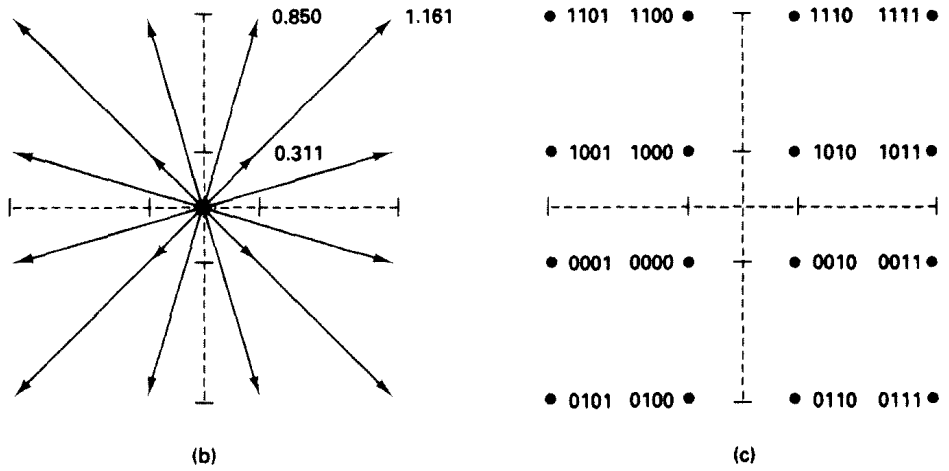
$$\text{summer output} = -0.22 \sin \omega_c t - 0.22 \cos \omega_c t$$
$$= 0.311 \sin(\omega_c t - 135°)$$

For the remaining quadbit codes, the procedure is the same. The

results are shown in Figure 2-35.

Binary input				16-QAM output	
Q	Q′	I	I′		
0	0	0	0	0.311 V	−135°
0	0	0	1	0.850 V	−165°
0	0	1	0	0.311 V	−45°
0	0	1	1	0.850 V	−15°
0	1	0	0	0.850 V	−105°
0	1	0	1	1.161 V	−135°
0	1	1	0	0.850 V	−75°
0	1	1	1	1.161 V	−45°
1	0	0	0	0.311 V	135°
1	0	0	1	0.850 V	165°
1	0	1	0	0.311 V	45°
1	0	1	1	0.850 V	15°
1	1	0	0	0.850 V	105°
1	1	0	1	1.161 V	135°
1	1	1	0	0.850 V	75°
1	1	1	1	1.161 V	45°

(a)



(b) (c)

FIGURE 2-35 16-QAM modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram.

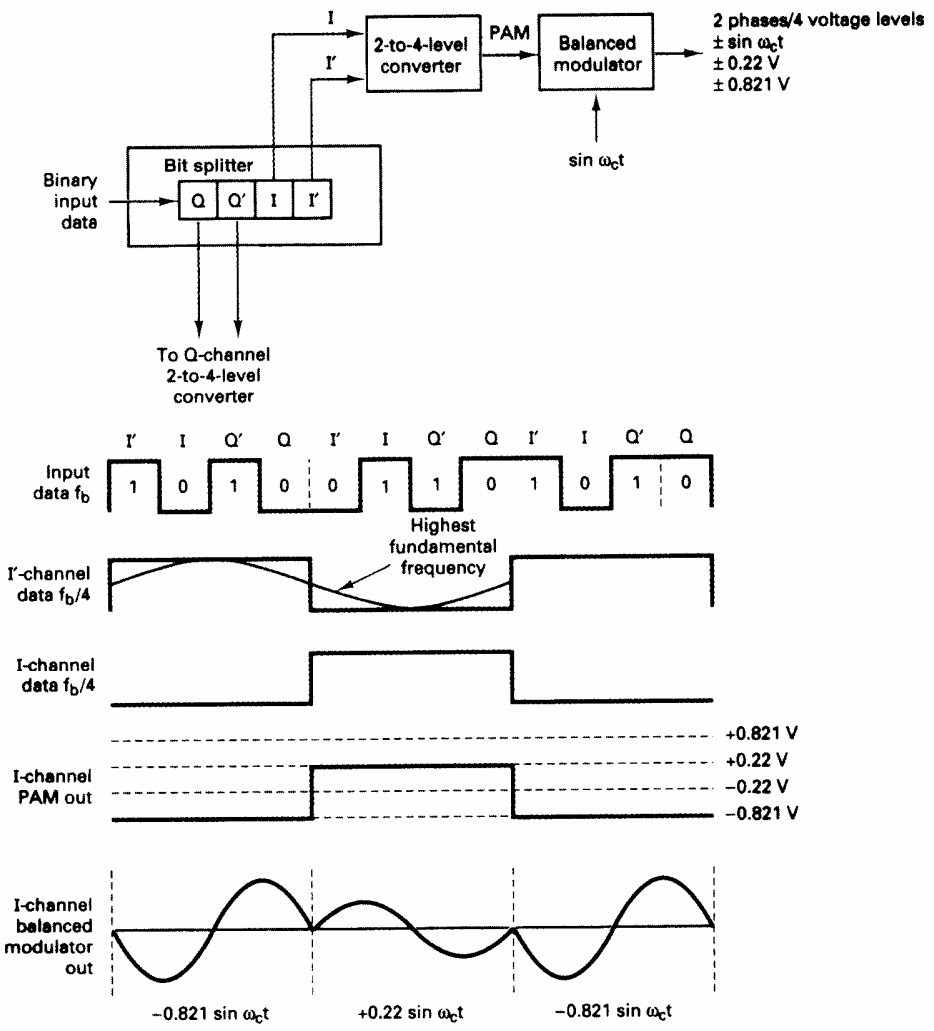


FIGURE 2-36 Bandwidth considerations of a 16-QAM modulator

2-6-2-2 Bandwidth considerations of 16-QAM.

With a 16-QAM, the bit rate in the I, I', Q, or Q' channel is equal to one-fourth of the binary input data rate ($f_b/4$).

Figure 2-36 shows the bit timing relationship between the binary input data; the I, I'. Q, and Q' channel data; and the I PAM signal. It can be seen that the highest fundamental frequency in the I, I', Q, or Q' channel is equal to one-eighth of the bit rate of the binary input data (one cycle in the I, I', Q, or

Q' channel takes the same amount of time as eight input bits). Also, the highest fundamental frequency of either PAM signal is equal to one-eighth of the binary input bit rate. With a 16-QAM modulator, there is one change in the output signal (either its phase, amplitude, or both) for every four input data bits. Consequently, the baud equals $f_b/4$, the same as the minimum bandwidth.

Again, the balanced modulators are product modulators and their outputs can be represented mathematically as

$$\text{output} = (X \sin \omega_a t)(\sin \omega_c t) \tag{2.26}$$

where

$$\underbrace{\omega_a t = 2\pi \frac{f_b}{8} t}_{\text{modulating signal}} \quad \text{and} \quad \underbrace{\omega_c t = 2\pi f_c t}_{\text{carrier}}$$

and

$$X = \pm 0.22 \text{ or } \pm 0.821$$

Thus,

$$\text{output} = \left(X \sin 2\pi \frac{f_b}{8} t\right)(\sin 2\pi f_c t)$$

$$= \frac{X}{2} \cos 2\pi \left(f_c - \frac{f_b}{8}\right) t = \frac{X}{2} \cos 2\pi \left(f_c + \frac{f_b}{8}\right) t$$

The output frequency spectrum extends from $f_c + f_b / 8$ and $f_c - f_b / 8$ the minimum bandwidth (f_N) is

$$\left(f_c + \frac{f_b}{8}\right) - \left(f_c - \frac{f_b}{8}\right) = \frac{2f_b}{8} = \frac{f_b}{4}$$

Example 2-11

For a 16-QAM modulator with an input data rate (f_b) equal to 10 Mbps and a carrier frequency of 70 MHz, determine the minimum double-sided Nyquist frequency (f_N) and the baud. Also, compare the results with those achieved with the BPSK, QPSK, and 8-PSK modulators in Examples 2-4, 2-6, and 2-8. Use the 16-QAM block diagram shown in Figure 2-33 as the modulator model.

Solution

The bit rate in the I, I', Q, and Q' channels is equal to one-fourth of the input bit rate,

$$f_{bI} = f_{bI'} = f_{bQ} = f_{bQ'} = f_b / 4 = 10 \text{ Mbps} / 4 = 2.5 \text{ Mbps}$$

Therefore, the fastest rate of change and highest fundamental frequency presented to either balanced modulator is

$$f_a = f_{bI} / 2 = 2.5 \text{ Mbps} / 2 = 1.25 \text{ MHz}$$

The output wave from the balanced modulator is

$$(\sin 2\pi f_a t)(\sin 2\pi f_c t)$$

$$0.5 \cos 2\pi(f_c - f_a)t - 0.5 \cos 2\pi(f_c + f_a)t$$

$$0.5 \cos 2\pi[(70 - 1.25)\text{MHz}]t - 0.5 \cos 2\pi[(70 + 1.25)\text{MHz}]t$$

$$0.5 \cos 2\pi(68.75\text{MHz})t - 0.5 \cos 2\pi(71.25\text{MHz})t$$

The minimum Nyquist bandwidth is

$$B=(71.25 - 68.75)\ MHz = 2.5\ MHz$$

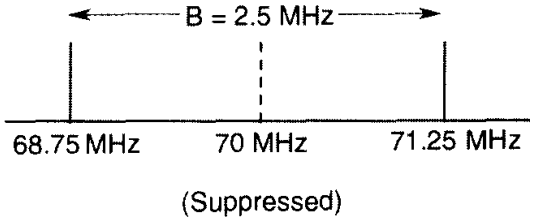
The minimum bandwidth for the 16-QAM can also be determined by simply substituting into Equation 2-10:

$$B = 10\ Mbps / 4 = 2.5\ MHz.$$

The symbol rate equals the bandwidth; thus,

symbol rate = 2.5 megabaud

The output spectrum is as follows:



For the same input bit rate, the minimum bandwidth required to pass the output of a 16-QAM modulator is equal to one-fourth that of the BPSK modulator, one-half that of QPSK, and 25% less than with 8-PSK. For each modulation technique, the baud is also reduced by the same proportions.

Example 2-12

For the following modulation schemes, construct a table showing the number of bits encoded, number of output conditions, minimum bandwidth, and baud for an information data rate of 12 kbps: QPSK, 8-PSK, 8-QAM, 16-PSK, and 16-QAM.

Modulation	n	M	B (Hz)	baud
QPSK	2	4	6000	6000
8-PSK	3	8	4000	4000
8-QAM	3	8	4000	4000
16-PSK	4	16	3000	3000
16-QAM	4	16	3000	3000

From Example 2-12, it can be seen that a 12-kbps data stream can be propagated through a narrower bandwidth using either 16-PSK or 16-QAM than with the lower levels of encoding.

Table 2-1 summarizes the relationship between the number of bits encoded, the number of output conditions possible, the minimum bandwidth, and the baud for ASK, FSK. PSK, and QAM.

When data compression is performed, higher data transmission rates are possible for a given bandwidth.

Table 2-1 ASK, FSK, PSK AND QAM summary.

Modulation	Encoding Scheme	Outputs Possible	Minimum Bandwidth	Baud
ASK	Single bit	2	f_b	f_b
FSK	Single bit	2	f_b	f_b
BPSK	Single bit	2	f_b	f_b
QPSK	Dibits	4	$f_b/2$	$f_b/2$
8-PSK	Tribits	8	$f_b/3$	$f_b/3$
8-QAM	Tribits	8	$f_b/3$	$f_b/3$
16-QAM	Quadbits	16	$f_b/4$	$f_b/4$
16-PSK	Quadbits	16	$f_b/4$	$f_b/4$
32-PSK	Five bits	32	$f_b/5$	$f_b/5$
32-QAM	Five bits	32	$f_b/5$	$f_b/5$
64-PSK	Six bits	64	$f_b/6$	$f_b/6$
64-QAM	Six bits	64	$f_b/6$	$f_b/6$
128-PSK	Seven bits	128	$f_b/7$	$f_b/7$
128-QAM	Seven bits	128	$f_b/7$	$f_b/7$

Note: f_b indicates a magnitude equal to the input bit rate.

2-7 BANDWIDTH EFFICIENCY

Bandwidth efficiency (sometimes called *information density* or *spectral efficiency*, often used to compare the performance of one digital modulation technique to another.

Mathematical bandwidth efficiency is

$$B\eta = \frac{transmission\ bit\ rate\ (bps)}{\min imum\ bandwidth\ (Hz)} = \frac{bits/s}{Hertz} \qquad (2.27)$$

Where $B\eta$ = bandwidth efficiency

Example 2-13

For an 8-PSK system, operating with an information bit rate of 24 kbps, determine (a) baud, (b) minimum bandwidth, and (c) bandwidth efficiency.

Solution

a. Baud is determined by substituting into Equation 2-10,

baud = 24 kbps / 3 = 8000

b. Bandwidth is determined by substituting into Equation 2-11:

B = 24 kbps / 3 = 8000

c. Bandwidth efficiency is calculated from Equation 2-27:

$B\eta$ = 24, 000 / 8000
= 3 bits per second per cycle of bandwidth

Example 2-14

For 16-PSK and a transmission system with a 10 kHz bandwidth, determine the maximum bit rate.

Solution

The bandwidth efficiency for 16-PSK is 4, which means that four bits can be propagated through the system for each hertz of bandwidth. Therefore, the maximum bit rate is simply the product of the bandwidth and the bandwidth efficiency, or

$$\text{bit rate} = 4 \times 10{,}000 = 40{,}000 \text{ bps}$$

Table 2-2 ASK, FSK, PSK and QAM summary

Modulation	Encoding Scheme	Outputs Possible	Minimum Bandwidth	Baud	Bη
ASK	Single bit	2	f_b	f_b	1
FSK	Single bit	2	f_b	f_b	1
BPSK	Single bit	2	f_b	f_b	1
QPSK	Dibits	4	$f_b/2$	$f_b/2$	2
8-PSK	Tribits	8	$f_b/3$	$f_b/3$	3
8-QAM	Tribits	8	$f_b/3$	$f_b/3$	3
16-PSK	Quadbits	16	$f_b/4$	$f_b/4$	4
16-QAM	Quadbits	16	$f_b/4$	$f_b/4$	4
32-PSK	Five bits	32	$f_b/5$	$f_b/5$	5
64-QAM	Six bits	64	$f_b/6$	$f_b/6$	6

Note: f_b indicates a magnitude equal to the input bit rate.

2-8 DIFFERENTIAL PHASE-SHIFT KEYING

Differential phase-shift keying (DPSK) is an alternative form of digital modulation where the binary input information is contained in the difference between two successive signaling elements rather than the absolute phase.

2-8-1 Differential BPSK

2-8-1-I DBPSK transmitter.

Figure 2-37a shows a simplified block diagram of a

differential binary phase-shift keying (DBPSK) transmitter. An incoming information bit is XNORed with the preceding bit prior to entering the BPSK modulator (balanced modulator).

For the first data bit, there is no preceding bit with which to compare it. Therefore, an initial reference bit is assumed. Figure 2-37b shows the relationship between the input data, the XNOR output data, and the phase at the output of the balanced modulator. If the initial reference bit is assumed a logic 1, the output from the XNOR circuit is simply the complement of that shown.

In Figure 2-37b, the first data bit is XNORed with the reference bit. If they are the same, the XNOR output is a logic 1; if they are different, the XNOR output is a logic 0. The balanced modulator operates the same as a conventional BPSK modulator; a logic I produces $+\sin \omega_c t$ at the output, and a logic 0 produces $-\sin \omega_c t$ at the output.

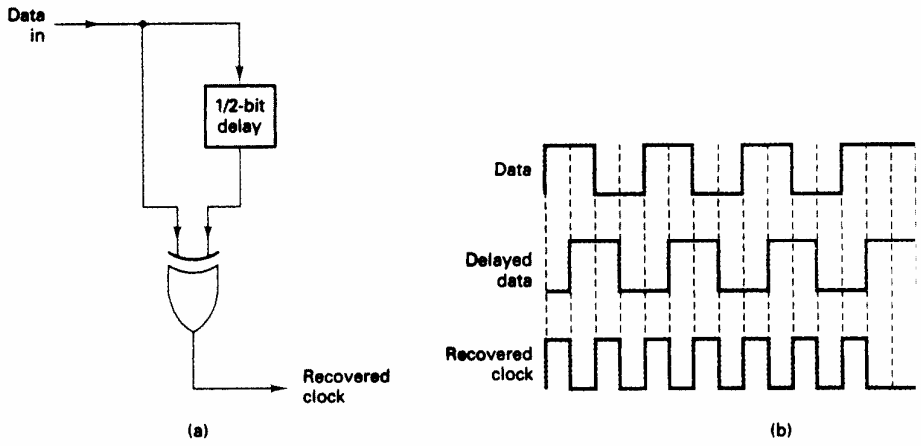


FIGURE 9-40 (a) Clock recovery circuit; (b) timing diagram

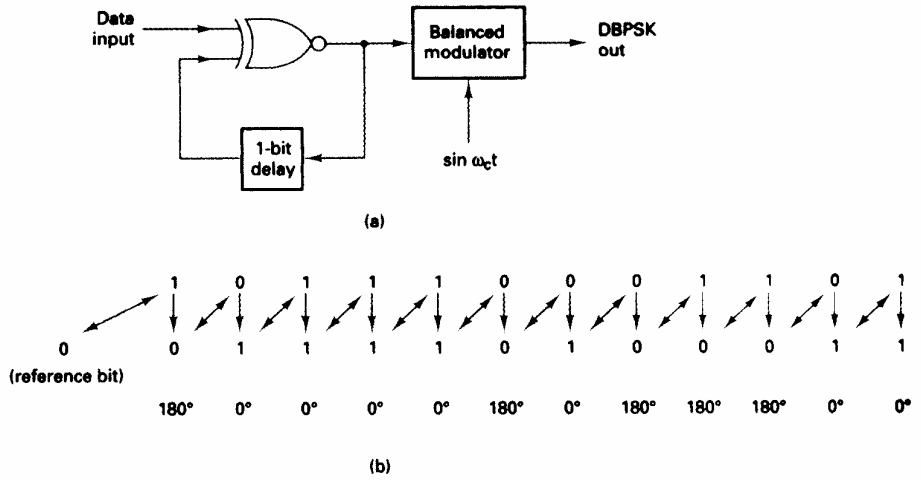


FIGURE 2-37 DBPSK modulator (a) block diagram (b) timing diagram

2-8-1-2 DBPSK receiver.

Figure 9-38 shows the block diagram and timing sequence for a DBPSK receiver. The received signal is delayed by one bit time, then compared with the next signaling element in the balanced modulator. If they are the same. J logic 1(+ voltage) is generated. If they are different, a logic 0 (- voltage) is generated. [f the reference phase is incorrectly assumed, only the first demodulated bit is in error. Differential encoding can

be implemented with higher-than-binary digital modulation schemes, although the differential algorithms are much more complicated than for DBPS K.

The primary advantage of DBPSK is the simplicity with which it can be implemented. With DBPSK, no carrier recovery circuit is needed. A disadvantage of DBPSK is, that it requires between 1 dB and 3 dB more signal-to-noise ratio to achieve the same bit error rate as that of absolute PSK.

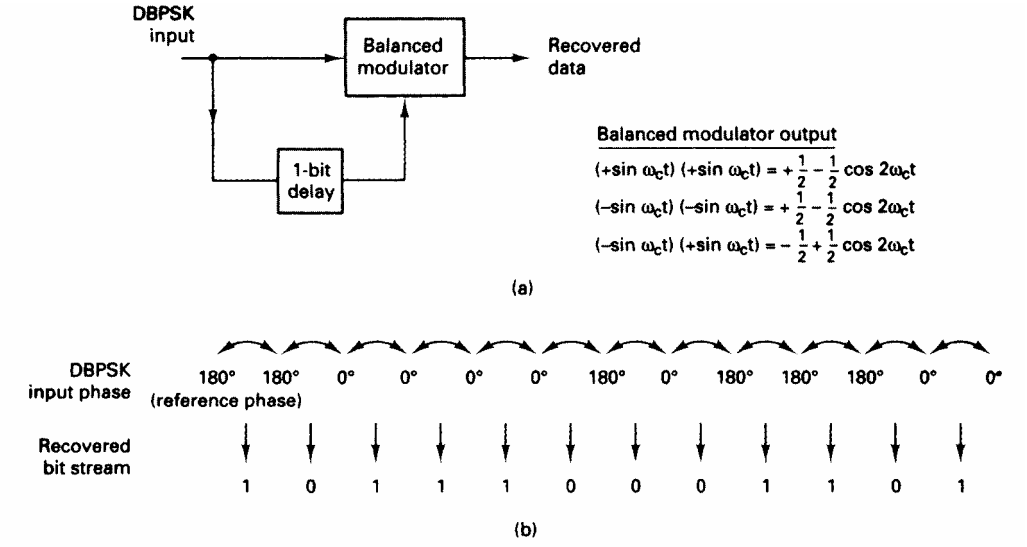


FIGURE 2-38 DBPSK demodulator: (a) block diagram; (b) timing sequence

2-9 PROBABILITY OF ERROR AND BIT ERROR RATE

Probability of error P(e) and *bit error rate* (BER) are often used interchangeably

BER is an empirical (historical) record of a system's actual bit error performance.

For example, if a system has a BER of 10^{-5}, this means that in past performance there was one bit error for every

100,000 bits transmitted.

Probability of error is a function of the *carrier-to-noise power ratio* (or, more specifically, the average *energy per bit-to-noise power density ratio)* and the number of possible encoding conditions used (M-ary).

Carrier-to-noise power ratio is the ratio of the average carrier power (the combined power of the carrier and its associated sidebands) to the *thermal noise power* Carrier power can be stated in watts or dBm. where

$$C_{(dBm)} = 10 \log [C_{(watts)} / 0.001] \quad (2.28)$$

Thermal noise power is expressed mathematically as

$$N = KTB \text{ (watts)} \quad (2.29)$$

where
N **=** thermal noise power (watts)
K = Boltzmann's proportionality constant ($1.38 X 10^{-23}$ joules per kelvin)
T= temperature (kelvin: 0 K=-273° C, room temperature = 290 K)
B = bandwidth (hertz)

Stated in dBm, $N_{(dBm)} = 10 \log [KTB / 0.001]$ (2.30)

Mathematically, the carrier-to-noise power ratio is

$$C / N = C / KTB \text{ (unitless ratio)} \quad (2.31)$$

where

C = carrier power (watts)

N = noise power (watts)

Stated in dB, $C / N\ (dB) = 10 \log [C / N]$

$$= C_{(dBm)} - N_{(dBm)} \qquad (2.32)$$

Energy per bit is simply the energy of a single bit of information. Mathematically, energy per bit is

$$E_b = CT_b\ (J/bit) \qquad (2.33)$$

where

E_b = energy of a single bit (joules per bit)
T_b = time of a single bit (seconds)
C = carrier power (watts)

Stated in dBJ, $E_{b(dBJ)} = 10 \log E_b \qquad (2.34)$

and because $T_b = 1/f_b$, where f_b is the bit rate in bits per second, E_b can be rewritten as

$$E_b = C / f_b\ (J/bit) \qquad (2.35)$$

Stated in dBJ, $E_{b(dBJ)} = 10 \log C / f_b \qquad (2.36)$

$$= 10 \log C - 10 \log f_b \qquad (2.37)$$

Noise power density is the thermal noise power normalized to a 1-Hz bandwidth (i.e., the noise power present in a 1-Hz bandwidth). Mathematically, noise power density is

$$N_o = N / B\ (W/Hz) \qquad (2.38)$$

where

N_o = noise power density (watts per hertz)
N = thermal noise power (watts)
B = bandwidth (hertz)

Stated in dBm, $N_{o(dBm)} = 10 \log (N/0.001) - 10 \log B$ (2.39)

Combining Equations 2.29 and 2.38 yields

$$N_o = KTB / B = KT \text{ (W/ Hz)} \quad (2.41)$$

Stated in dBm, $N_{o(dBm)} = 10 \log (K/0.001) + 10 \log T$ (2.42)

Energy per bit-to-noise power density ratio is used to compare two or more digital modulation systems that use different transmission rates (bit rates), modulation schemes (FSK, PSK, QAM), or encoding techniques (M-ary).

Mathematically, E_b/N_o is

$$E_b/N_o = (C/f_b) / (N/B) \quad (2.43)$$

where E_b/N_o *is* the energy per bit-to-noise power density ratio. Rearranging Equation 2.43 yields the following expression:

$$E_b/N_o = (C/N) \times (B/f_b) \quad (2.44)$$

where
E_b/N_o = energy per bit-to-noise power density ratio
C/N = carrier-to-noise power ratio
B/f_b = noise bandwidth-to-bit rate ratio

Stated in dB, $E_b/N_o\ (dB) = 10 \log (C/N) + 10 \log (B/f_b)$ (2.45)

$$= 10 \log E_b - 10 \log N_o \qquad (2.46)$$

Example 2-15

For a QPSK system and the given parameters, determine
a. Carrier power in dBm.
b. Noise power in dBm.
c. Noise power density in dBm.
d. Energy per bit in dBJ.
e. Carrier-to-noise power ratio in dB.
f.. $E_b lN_o$ ratio.

$C = 10^{-12}$ W
$F_b = 60$ kbps
$N = 1.2 \times 10^{-14}$W
$B = 120$ kHz

Solution

a. The carrier power in dBm is determined by substituting into Equation 2.28:

$$C = 10 \log (10^{-12} / 0.001) = - 90 \text{ dBm}$$

b. The noise power in dBm is determined by substituting into Equation 2-*30:*

$$N = 10 \log [(1.2 \times 10^{-14}) / 0.001] = -109.2 \text{ dBm}$$

c. The noise power density is determined by substituting into Equation 2-*40:*

$$N_o = -109.2 \text{ dBm} - 10 \log 120 \text{ kHz} = -160 \text{ dBm}$$

d. The energy per bit is determined by substituting into equation

2.36:

$$E_b = 10 \log (10^{-12} / 60 \text{ kbps}) = -167.8 \text{ dBJ}$$

e. The carrier-to-noise power ratio is determined by substituting into Equation *2.34:*

$$C / N = 10 \log (10^{-12} / 1.2 \times 10^{-14}) = 19.2 \text{ dB}$$

f. The energy per bit-to-noise density ratio is determined by substituting into Equation *2.45:*

$$E_b / N_o = 19.2 + 10 \log 120 \text{ kHz} / 60 \text{ kbps} = 22.2 \text{ dB}$$

2-10 ERROR PERFORMANCE

2-10-1 PSK Error Performance

The bit error performance is related to the distance between points on a signal state-space diagram.

For example, on the signal state-space diagram for BPSK shown in Figure 2.39a, it can be seen that the two signal points (logic 1 and logic 0) have maximum separation *(d)* for a given power level (D).

The figure shows, a noise vector (V_N), when combined with the signal vector (V_s), effectively shifts the phase of the signaling element (V_{SE}) alpha degrees.

If the phase shift exceeds +90°, the signal element is shifted beyond the threshold points into the error region.

For BPSK, it would require a noise vector of sufficient amplitude and phase to produce more than a ±90° phase shift in the signaling element to produce an error.

For PSK systems, the general formula for the threshold points is

$$TP = \pm \pi / M \qquad (2.47)$$

where M is the number of signal states.

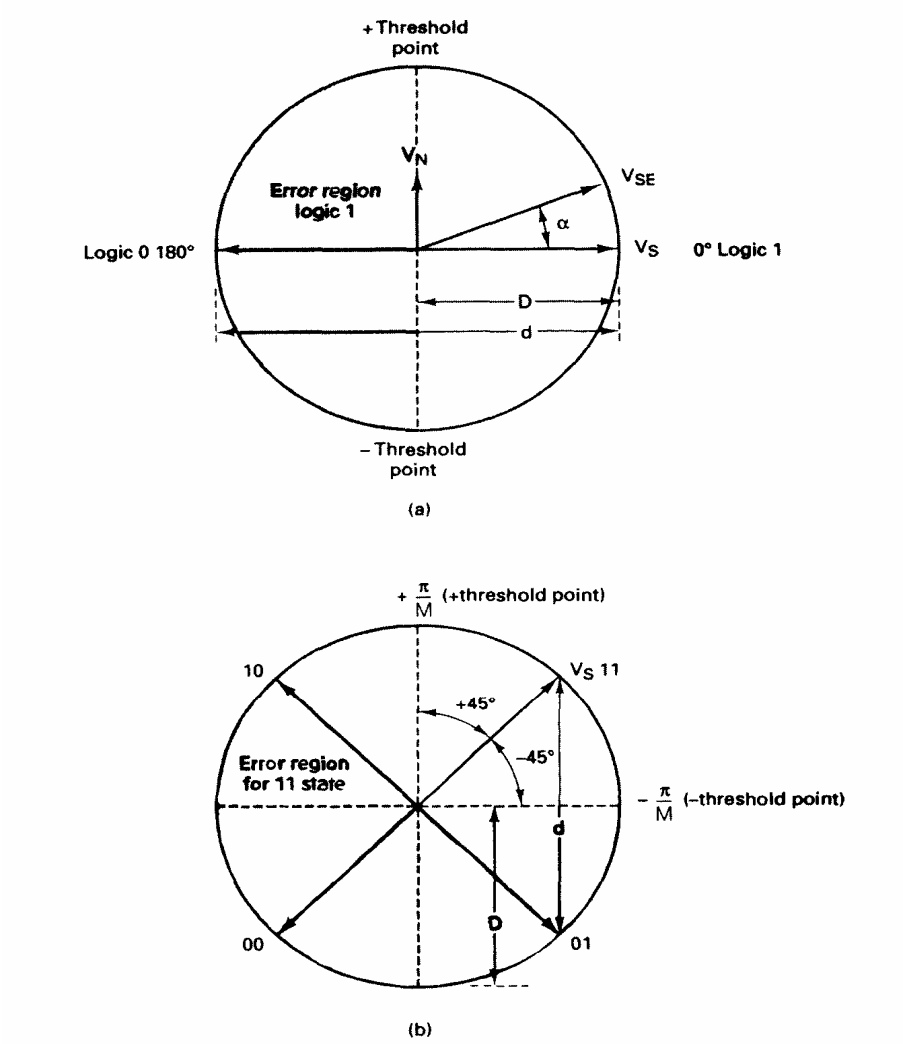


FIGURE 2-39 PSK error region: (a) BPSK; (b) QPSK

The phase relationship between signaling elements for BPSK (i.e., 180^0 out of phase) is the optimum signaling format, referred to as *antipodal signaling,* and occurs only when two binary signal levels are allowed and when one signal is the exact negative of the other. Because no other bit-by-bit signaling scheme is any better, antipodal performance is often used as a reference for comparison.

The error performance of the other multiphase PSK systems can be compared with that of BPSK simply by determining the relative decrease in error distance between points on a signal state-space diagram.

For PSK, the general formula for the maximum distance between signaling points is given by

$$\text{Sin } \theta = \sin 360^0 / 2M = (d/2) /D \qquad (2.48)$$

d = error distance
M = number of phases
D = peak signal amplitude

Rearranging equation 2.48 and solving for *d* yields

$$d = \left(2 \sin \frac{180^0}{M}\right) xD \qquad (2.49)$$

Figure 2-39b shows the signal state-space diagram for QPSK. From Figure 2-39 and Equation 2.48, it can be seen that QPSK can tolerate only a ± 45° phase shift.

From Equation 2.47 the maximum phase shift for 8-PSK and 16-PSK is ±22.5° and ±11.25°, respectively.

The higher the level of modulation, the smaller the angular separation between signal points and the smaller the error distance.

The general expression for the bit error probability of an M-phase PSK system is

$$P(e) = (1 / \log_2 M) \text{ erf } (z) \qquad (2.50)$$

where erf = error function

$$z = \sin(\pi/M)\ (\sqrt{\log_2 M})(\sqrt{E_b / N_0})$$

By substituting into Equation 2.50, it can be shown that QPSK provides the same error performance as BPSK. This is because the 3-dB reduction in error distance for QPSK is offset by the 3-dB decrease in its bandwidth (in addition to the error distance, the relative widths of the noise bandwidths must also be considered).

Thus, both systems provide optimum performance. Figure 2-40shows the error performance for 2-4-, 8-, 16-, and 32-PS K systems as a function of E_b / N_o.

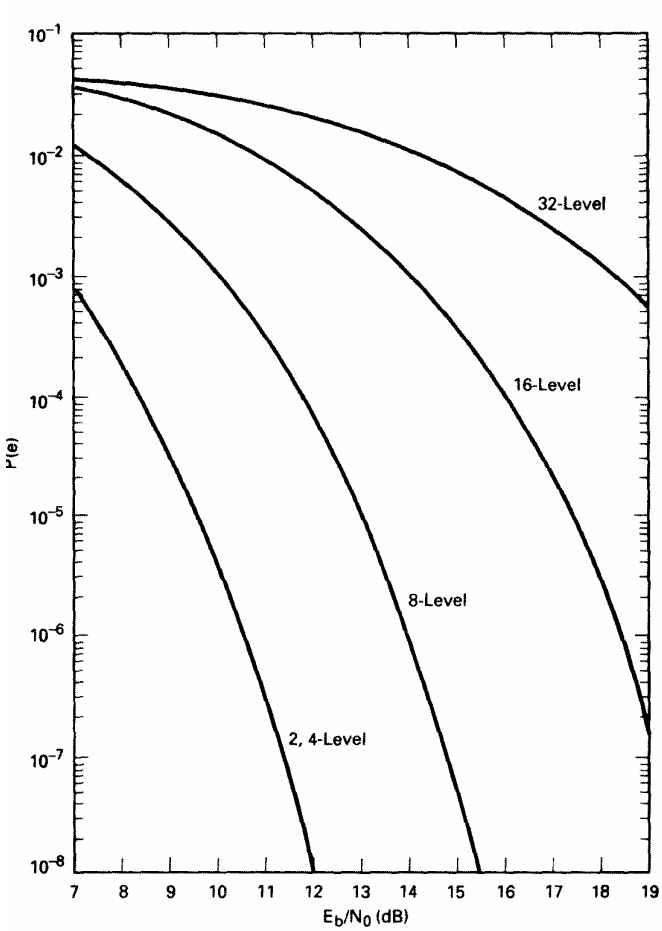


FIGURE 2-40 Error rates of PSK modulation systems

Example 2-16

Determine the minimum bandwidth required to achieve a *P(e)* of 10^{-7} for an 8-PSK system operating at 10 Mbps with a carrier-to-noise power ratio of 11.7 dB.
Solution

From Figure 2-40, the minimum E_b / N_o ratio to achieve a *P(e)* of 10^{-7} for an 8-PSK system is 14.7 dB. The minimum bandwidth is found by rearranging Equation 2.44:

$$B / f_b = E_b / N_o = C / N$$

$$= 14.7 \text{ dB} - 11.7 \text{ dB} = 3 \text{ dB}$$

$$B / f_b = \text{antilog } 3 = 2 \text{ ; } B = 2 \times 10 \text{ Mbps} = 20 \text{ MHz}$$

2-10-2 QAM Error Performance

For a large number of signal points (i.e., M-ary systems greater than 4), QAM outperforms PSK. This is because the distance between signaling points in a PSK system is smaller than the distance between points in a comparable QAM system. The general expression for the distance between adjacent signaling points for a QAM system with L levels on each axis is

$$d = \frac{\sqrt{2}}{L-1} D \quad (2.51)$$

where d = error distance
L = number of levels on each axis
$\boldsymbol{D}$ = peak signal amplitude

In comparing Equation 2-49 to Equation 2-5 1, it can be seen that QAM systems have an advantage over PSK systems with the same peak signal power level. The general expression for the bit error probability of an L-level QAM system is

$$P(e) = \frac{1}{\log_2 L}\left(\frac{L-1}{L}\right) erfc(z)$$

(2.52)

Where erfc(z) is the complementary error function

Figure 2-41 shows the error performance for 4-, 16-, 32-, and 64-QAM systems as a function of E_b/N_o.

Table 2-4 lists the minimum carrier-to-noise power ratios and energy per bit-to-noise power density ratios required for a probability of error 10^{-6} for several PSK and QAM modulation schemes.

Example 2-17

Which system requires the highest E_b/N_o ratio for a probability of error of 10^{-6} , a four-level QAM system or an 8-PSK system?

Solution

From Figure 2-41, the minimum E_b/N_O ratio required for a four-level QAM system is, 10.6 dB. From Figure 2-40, the minimum E_b/N_o ratio required for an 8-PSK system is 14 dB Therefore, to achieve *a P(e)* of 10^{-6}, a four-level QAM system would require 3.4 dB less E_b/N_O ratio.

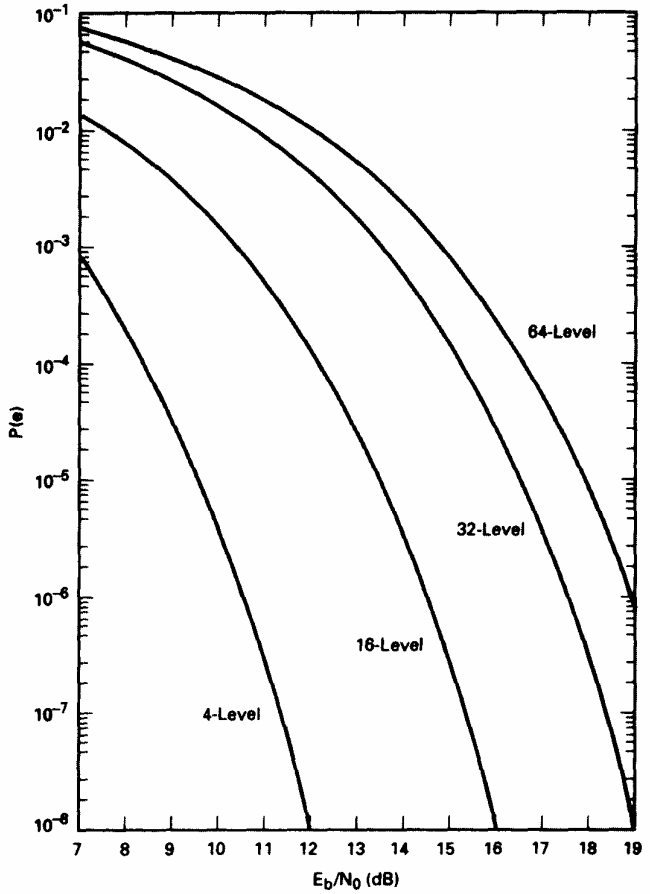


FIGURE 2-41 Error rates of QAM modulation systems.

Table 2-4 Performance Comparison of various digital modulation schemes (BER = 10^{-6})

Modulation Technique	C/N Ratio (dB)	E_b/N_0 Ratio (dB)
BPSK	10.6	10.6
QPSK	13.6	10.6
4-QAM	13.6	10.6
8-QAM	17.6	10.6
8-PSK	18.5	14
16-PSK	24.3	18.3
16-QAM	20.5	14.5
32-QAM	24.4	17.4
64-QAM	26.6	18.8

2-10-3 FSK Error Performance

With noncoherent FSK, the transmitter and receiver are not frequency or phase synchronized. With coherent FSK, local

receiver reference signals are in frequency and phase lock with the transmitted signals. The probability of error for noncoherent FSK is

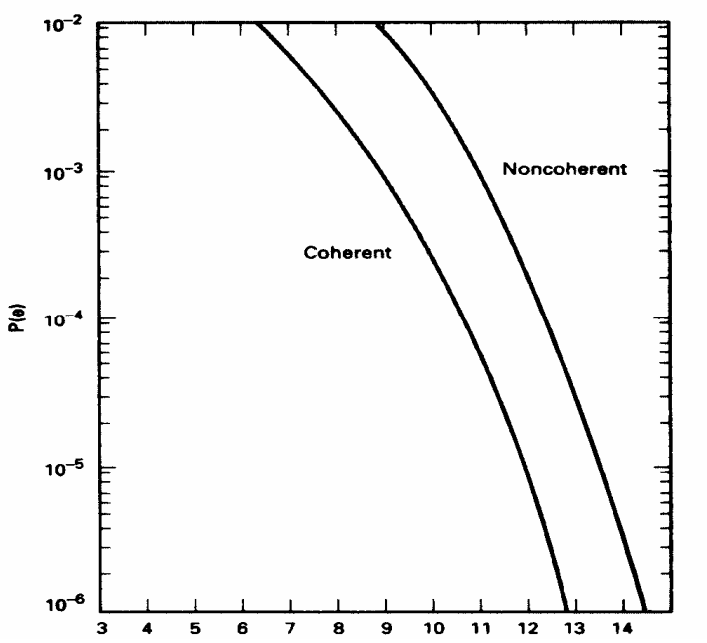


FIGURE 2-42 Error rates for FSK modulation systems

$$P(e) = 1/2 \exp\left(\frac{-E_b}{2N_o}\right) \tag{2.53}$$

The probability of error for coherent FSK is

$$P(e) = erfc\sqrt{\frac{E_b}{N_0}} \tag{2.54}$$

Figure 2-42 shows probability of error curves for both coherent and noncoherent FSK for several values of E_b/N_o. From Equations 2-53 and 2-54, it can be determined that the probability of error for noncoherent FSK is greater than that of coherent FSK for equal energy per bit-to-noise power density ratios.